SC2021A Type-C/ PD and Dual DPDM Fast Charge Controller

1 Description

SC2021A is a Type-C / PD and DPDM fast charge controller. It complies with the latest Type-C and PD 3.0 standards and supports the proprietary high voltage fast charge protocols with dual DPDM interfaces. It targets for the wall adapters, travel adapters and car chargers.

SC2021A minimizes external components by integrating USB PD baseband PHY, Type-C detection, dual DPDM PHYs, VBUS discharging paths, VCONN supply, programmable feedback compensation, voltage and current sense, 10-bit high performance ADC, dual 10-bit DACs, NMOS gate driver, I2C interface and protection circuits. It contains a 32-bit high performance micro-controller core with 32kByte MTP ROM and 2.5kByte RAM, which provides cost effective solutions to many applications.

SC2021A supports various protection mechanisms including Over Voltage Protection (OVP), Under Voltage Protection (UVP), Over Current Protection (OCP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), DPDM Over Voltage Protection (DPDM OVP), CC Over Voltage Protection (CCOVP), VCONN Over Voltage (VCONN OVP), VCONN Over Current (VCONN OCP) and VCONN Short Protection (VCONN SCP), so to effectively ensure stable and reliable operation of system.

The SC2021A is available in 32-pin QFN package.

2 Features

- **USB Type-C**
  - Support Type-C DFP protocols
  - Configurable resistor R_P
- **USB Power Delivery**
  - Support DFP USB PD 3.0 with PPS
  - Hardware BMC transmitter and receiver
  - Full feature physical layer
  - Hardware CRC
  - Hardware reset
  - Integrate PD 3.0 protocol engine
  - Integrate VCONN and support SOP' for e-marker
- **Dual DPDM Fast Charging Interfaces**
  - Integrate 2x firmware controlled DPDM interfaces
  - Support Apple charging, BC1.2, DCP, HVDCP, FC, AFC, FCP, SCP, VOOC, UART, I2C and other proprietary charging protocols
- **Power**
  - Wide operation range: 3.05V to 22V (26V tolerant)
  - Integrate programmable feedback compensation
- **MCU Subsystem**
  - Integrated 32-bit high performance MCU core
  - 32kByte MTP and 2.5kByte RAM
  - Reserve independent space for storing chip ID code
  - Support UART, I2C and multiple I/Os
  - Support sleep mode
- **Analog Block**
  - Support OPTO interface for adapter
  - Support FB interface for car charger
  - Dual DACs for CC/CV loop.
  - 10-bit ADC to monitor the voltage / current / DPDM/ other signals
  - Integrated high side current sense amplifier
  - Integrated NMOS gate driver
  - Integrated VBUS discharging paths
  - Integrated temperature sense module
- **Protections**
  - 26V tolerant for CC1 and CC2
  - 12V tolerant for DP and DM
  - On chip OVP, UVP, SCP, VCONN OVP, VCONN OCP, VCONN SCP, OTP, DPDM OVP, CC OVP
- **Package**
  - 32-pin QFN, 4mm x 4mm x 0.75mm

3 Applications

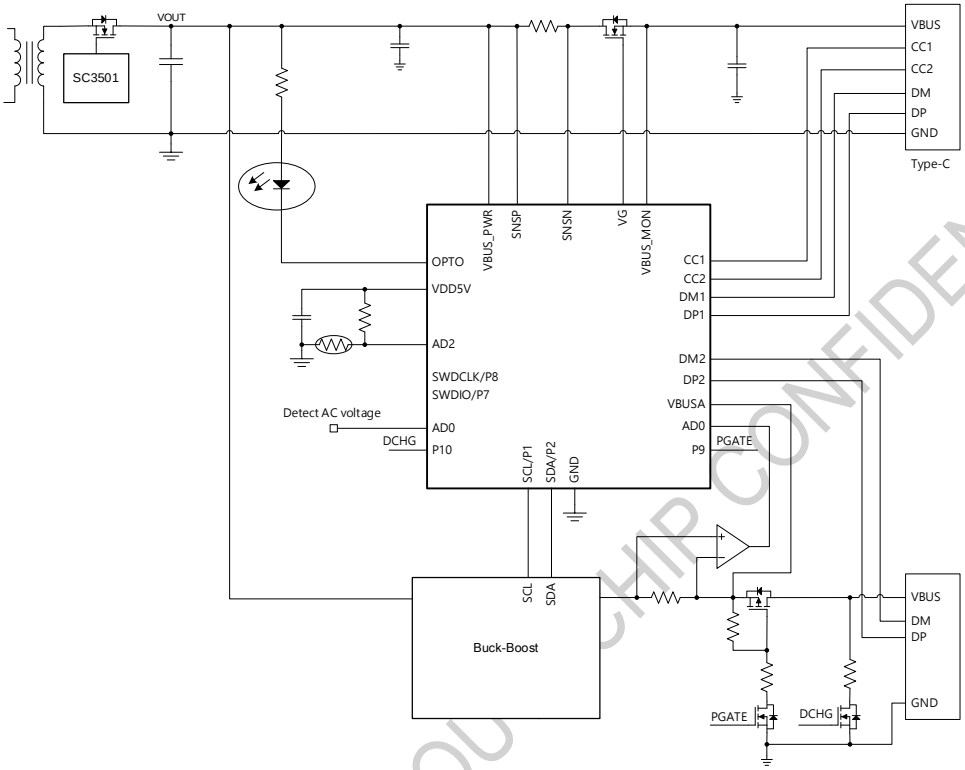
- Wall adapters
- Travel adapters
- Car chargers

4 Device Information

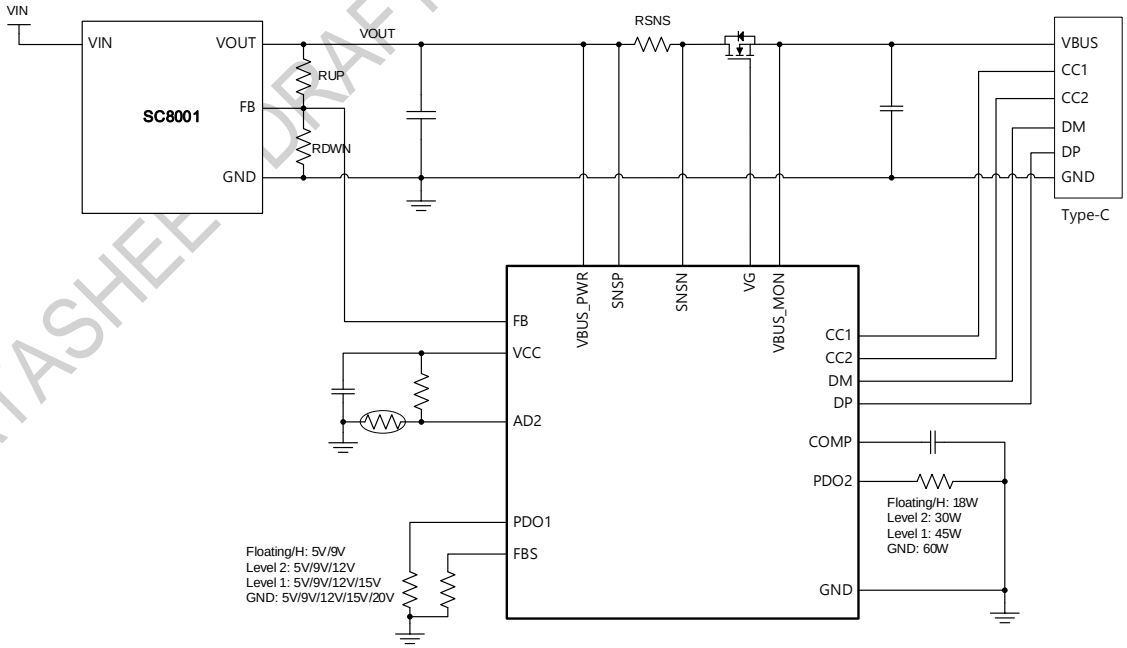
Part Number	Package	Body Size
SC2021AQDER	QFN32	4mm x 4mm x 0.75mm

5 Typical Application Diagram

QFN-32 Application-1 Diagram

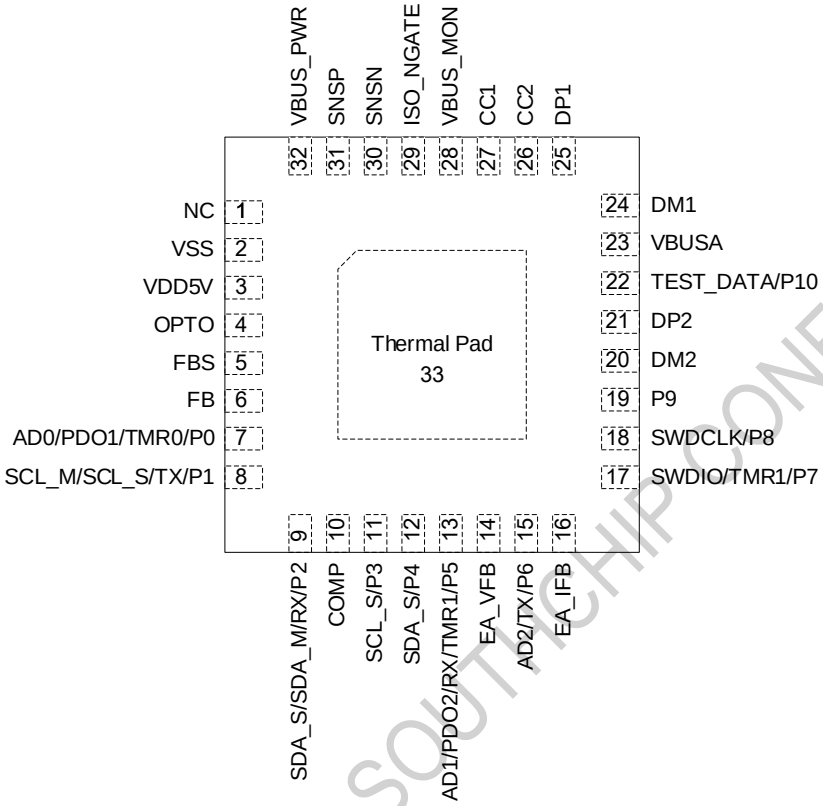


QFN-32 Application-2 Diagram



6 Terminal Configuration and Functions

TOP VIEW of SC2021A (QFN-32)



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	NC	-	No connect
2	VSS	I/O	Ground of IC
3	VDD5V	O	Output of 5V LDO. Provide power supply for internal circuits. Connect a 2.2uF capacitor to ground
4	OPTO	I	Current sink output for optocoupler connection
5	FBS	I	This pin is used to set the bias current when FB control is used to adjust the output voltage of power IC. Connect a resistor between this pin and ground. Leave this pin floating if FB control is not used
6	FB	I	If FB control is adopted to adjust the output voltage of the power IC, connect this pin to the feedback divider of the power IC. If FB control is not adopted, leave this pin floating or use this pin as GPIO
7	AD0	I	A/D converter input channel 0
	PDO1	I	Power data object setting pin1. Connect a resistor from this pin to ground for firmware setting the output voltage

	TMR0	O	Timer0 output. When configured as timer0 output, this pin shall toggle once timer0 counter counts to zero
	P0	I/O	General purpose IO
8	SCL_M	O	I2C master interface clock line
	SCL_S	O	I2C slave interface clock line
	TX	O	Transmit port when configure as UART interface
	P1	I/O	General purpose IO
9	SDA_M	I/O	I2C master interface data line
	SDA_S	I/O	I2C slave interface data line
	RX	I	Receive port when configure as UART interface
	P2	I/O	General purpose IO
10	COMP	I/O	If FB control is adopted to adjust the output voltage of the power IC, connect a capacitor to this pin to compensate CC loop
11	SCL_S	I	I2C slave interface clock
	P3	I/O	General purpose IO
12	SDA_S	I/O	I2C slave interface data
	P4	I/O	General purpose IO
13	AD1	I	A/D converter input channel 0
	PDO2	I	Power data object setting pin2. Connect a resistor from this pin to ground for firmware setting the output power
	RX	I	Receive data in when configure as UART interface
	TMR1	O	Timer1 output. When configured as timer1 output, this pin shall toggle once timer1 counter counts to zero
	P5	I/O	General purpose IO
14	EA_VFB	I/O	Constant voltage loop EA compensation pin
15	AD2	I	A/D converter input channel 0
	TX	O	Transmit when configure as UART interface
	P6	I/O	General purpose IO
16	EA_IFB	I/O	Constant current loop EA compensation pin
17	SWDIO	I/O	Debug data line

	TMR1	O	Timer1 output. When configured as timer1 output, this pin shall toggle once timer1 counter counts to zero
	P7	I/O	General purpose IO
18	SWDCLK	I	Debug clock line
	P8	I/O	General purpose IO
19	P9	I/O	General purpose IO
20	DM2	I/O	DM line of fast charging interface 2
21	DP2	I/O	DP line of fast charging interface 2
22	P10	I/O	General purpose IO
23	VBUSA	I	Connected to the VBUS line of the USB-A port. It can discharge the output capacitor and could be used to sense VBUS voltage of USB-A port
24	DM1	I/O	DM line of fast charging interface 1
25	DP1	I/O	DP line of fast charging interface 1
26	CC2	I/O	Type-C configure channel2. It also supports VCONN output
27	CC1	I/O	Type-C configure channel1. It also supports VCONN output
28	VBUS_MON	I	Connected to the VBUS line of the USB Type-C port. It can discharge the output capacitor and could be used to sense VBUS voltage of Type-C port
29	NGATE	O	Load switch (NMOS) driver
30	SNSN	I	Negative input of the internal current sense amplifier. Connect to the high side current sense resistor for the Type-C port
31	SNSP	I	Positive input of the internal current sense amplifier. Connect to the high side current sense resistor for the Type-C port
32	VBUS_PWR	I	IC supply input. It supports more than 100mA discharging capability for the internal VBUS capacitor and could be used to sense VBUS voltage
33	Thermal Pad	-	Connect this pad to VSS

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	ISO_NGATE	-0.3	31	V
	VBUS_PWR, VBUS_MON, SNSP, SNSN, CC1, CC2, OPTO, VBUSA	-0.3	26	V
	DP1, DM1, DP2, DM2	-0.3	12	V
	FB, AD0/PDO1/TMR0/P0, SCL_M/SCL_S/TX/P1, SDA_S/SDA_M/RX/P2, SCL_S/P3, SDA/P4, AD1/PDO2/RX/TMR1/P5, AD2/TX/P6, SWDIO/TMR1/P7, SWDCLK/TEST_SCL/P8, P9, P10, VDD5V, COMP, EA_VFB, EA_IFB, FBS	-0.3	5.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE (1)		QFN-16 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	TBD	℃/W
θ_{JC}	Junction to case thermal resistance	TBD	℃/W

7.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)	All pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{BUS_PWR}	VBUS_PWR operation voltage	3.05		22	V
C_{VBUS_PWR}	Bulk capacitor at VBUS_PWR pin			1600(1)	μF
C_{VBUS_MON}	Bulk capacitor at VBUS_MON pin	1		10	μF
C_{VDD5V}	Capacitor at VDD5V pin	2.2			μF

R_{SNS}	Sense resistor between CS+ and CS- pins	3	5	10	mΩ
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

(1) It is recommended to add external discharge circuit on VBUS_PWR, if the bulk capacitance at VBUS_PWR node is higher than 1600μF.

7.5 Electrical Characteristics

T_J= 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{BUS_PWR}	VBUS_PWR supply range		3.05		22	V
$V_{BUS\_PWR\_POR}$	VBUS_PWR power on threshold	VBUS_PWR rising threshold		2.9	3.05	V
$V_{BUS\_PWR\_UVLO}$	VBUS_PWR UVLO threshold	VBUS_PWR falling threshold	2.55	2.7		V
I_{q_ACT}	Quiescent current in active mode	VBUS_PWR=5V, MCU core is active		12		mA
I_{q_SBY}	Quiescent current in standby mode	VBUS_PWR=5V, standby mode, digital DPDM module wakes up, all analog peripherals enabled		2		mA
I_{q_SLEEP}	Quiescent current in sleep mode	Control loop disabled, MCU and peripherals all disabled except CC		160	200	µA
5V LDO						
V_{LDO_5V}	5V LDO regulation voltage	VBUS_PWR = 5.5V~20V	4.9	5	5.1	V
V_{LDO_DROP}	5V LDO drop out voltage	V_{BUS_PWR}-V_{LDO5V}, I_{OUT} = 50 mA			150	mV
I_{LDO_LIMIT}	LDO current limit	V_{BUS_PWR} = 5V	90	100	120	mA
DISCHARGE						
$I_{DIS\_VBUS\_PWR}$	Discharging current at VBUS_PWR	Register-Programmable	25		150	mA
$R_{DCHG\_VBUS\_MON}$	Discharging resistor at VBUS_MON			1	1.4	kΩ
R_{DCHG_VBUSA}	Discharging resistor at VBUSA			1	1.4	kΩ
NMOS GATE DRIVER						
V_{DRV}	Driving voltage	V_{GATE}-V_{BUS_MON}, VBUS_PWR ≥ 3.3V		5		V
V_{CLAMP_GS}	Driver clamp voltage	V_{GATE}-V_{BUS_MON}		7		V
R_{DRIVE_UP}	Driver pull up resistance	VBUS_PWR=5V, Register-Programmable	20		200	kΩ
CURRENT SENSE						
G_{CSNS}	Gain of current sense amplifier	cs_sel_20x = 1	19.8	20	20.2	
		cs_sel_20x = 0	39.6	40	40.4	
V_{OCP}	OCP threshold, calculated as I_{BUS}*R_{SNS}	cs_sel_vocp = 1		30	31	mV
		cs_sel_vocp = 0		36	37	mV
V_{OCP_DT}	OCP deglitch time			1000		µs
G_{LINE_COMP}		cs_ana_comp_clamp_dis = 1		0		

	VBUS output compensation respect to the output of CSNS amplifier	cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 00b		1/4		
		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 01b		1/2		
		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 10b		7/12		
		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 11b		5/6		
$V_{LINE\_COMP\_MAX}$	Max VBUS output voltage compensation		160	200	240	mV
ADC						
V_{ADC_REF}	Reference voltage for ADC		2.249	2.253	2.257	V
N_{ADC}	Resolution			10		Bits
R_{SAMPLE}	ADC sample rate	Register programable	47.5	50	52.5	ksps
			23.75	25	26.25	ksps
			9.5	10	10.5	ksps
			4.75	5	5.25	ksps
$K_{ADC\_VBUS\_PWR}$	Ratio from VBUS_PWR voltage sense			1/10		
$K_{ADC\_VBUS\_MON}$	Ratio from VBUS_MON voltage sense			1/10		
K_{ADC_VBUSA}	Ratio from VBUSA voltage sense			1/10		
K_{ADC_CSNS}	Ratio from the output of current sense amplifier			1		
K_{ADC_DPDM}	Ratio from DP1, DP2, DM1, DM2			1/4		
K_{ADC_VDD5V}	Ratio from VDD5V			1/4		
$K_{ADC\_0\_2}$	Ratio from ADC0, ADC1 or ADC2 voltage sense			1		
K_{ITC}	Internal temperature sense coefficient			2.819		mV/℃
$V_{ITC\_27℃}$	Internal temperature sense output at 27 ℃			733.94		mV
ADC_{VBUS_PWR}, ADC_{VBUS_MON}, ADC_{VBUSA}	Range		3.0		22.46	V
	LSB			22		mV
	Error	VBUS = 3.3V ~ 9V	-50		50	mV
		VBUS = 9V ~ 21V	-100		100	mV
ADC_{DPX}, ADC_{DMX}	Range		0		8.983	V
	LSB			8.78		mV
	Error	Full range	-150		150	mV

ADC_{ADX}, ADC_{CSNS}	Range		0		2.251	V
	LSB			2.2		mV
	Error	Full range	-5		5	mV
INL	Integral non-linearity		-1.0		1.0	LSB
DNL	Differential non-linearity		-1.0		1.0	LSB
OPTO CV-DAC and CC-DAC						
$R_{FB\_VBUS\_PWR}$	VBUS_PWR Divider Resistance	R_{UP} + R_{DWN} on VBUS_PWR pin	2			MΩ
K_V	Ratio from VBUS_PWR to the input of ADC.	Ratio from VBUS_PWR to the input of ADC		1/10		
N_{DAC_CV}	CV loop V_{REF} resolution			10		Bits
$V_{BUS\_PWR\_ADJ\_RANG}$	VBUS_PWR adjust range [1]		2		22.46	V
$V_{BUS\_PWR\_STEP\_VOLT}$	VBUS_PWR adjust voltage per step			20		mV
$V_{DAC\_ZERO\_VOLT}$	VBUS_PWR voltage at VDAC code = 0 [1]		1960	2000	2040	mV
N_{DAC_CC}	CC loop I_{REF} resolution			10		Bits
V_{REF_IDAC}	IDAC reference voltage			1.2		V
$V_{REF\_IDAC\_STEP}$	IDAC step voltage			1.172		mV
I_{REG_STEP}	Current regulation per step	RSNS=5mΩ, GSNS = 40×		5.86		mA
I_{VFB}	Current capability from VFB pin		-16		16	μA
I_{IFB}	Current capability from IFB pin		-16		16	μA
I_{OPTO}	OPTO control loop current		2			mA
FB CV-DAC AND CC-DAC						
$V_{FB\_VDAC\_REF}$	FB regulator VDAC reference			1.024		V
$V_{FB\_VDAC\_STEP}$	FB VDAC step voltage			1		mV
$V_{BUS\_PWR\_STEP\_VOLT\_FB}$	VBUS_PWR adjust voltage per step via FB	R_{UP} = 20×R_{FBS}		20		mV
I_{FB_SRC}	FB source capability	FB = 2.5V	400			μA
I_{FB_SNK}	FB sink capability	FB = 0.8V	400			μA
$V_{DCDC\_IDAC\_REF}$	DCDC regulator IDAC reference		2.244	2.248	2.252	mV
$I_{FB\_REG\_STEP}$	Output current regulation per step by DCDC IDAC			10.98		mA
I_{COMP}	Current capability from COMP pin		-4		2	μA
VBUS OVP and UVP						
$V_{BUS\_PWR\_OVP}$	VBUS_PWR OVP rising threshold	fb_sel_uvp_th = 01b	105	110	115	%
		fb_sel_uvp_th = 10b	110	115	121	%

		fb_sel_uvp_th = 11b	115	120	125	%
$V_{BUS\_OVP\_HYS}$	VBUS_PWR OVP threshold hysteresis, respect to VDAC setting			0	5	%
$t_{VBUS\_PWR\_OVP}$	VBUS_PWR over-voltage deglitch time	ovp_dgl_sel = 0		4		µs
		ovp_dgl_sel = 1		40		µs
$V_{BUS\_PWR\_UVP}$	VBUS_PWR UVP falling threshold	fb_sel_uvp_th = 01b	73	75	77	%
		fb_sel_uvp_th = 10b	82	85	88	%
		fb_sel_uvp_th = 11b	91	95	99	%
$V_{BUS\_UVP\_HYS}$	VBUS_PWR UVP threshold hysteresis, respect to VDAC setting			0	3	%
$t_{VBUS\_PWR\_OVP}$	UVP deglitch time	uvp_dgl_sel = 0		4		µs
		uvp_dgl_sel = 1		40		µs
$V_{BUS\_SCP\_TH}$	VBUS_PWR SCP threshold		3.1	3.2		V
t_{VMON_SCP}	VBUS_MON SCP deglitch time			0		µs
TYPE-C/ PD PROTOCOLS						
$I_{CC\_80µA}$	CC1/2 pull up current	CSRC_I = 00b	64	80	96	µA
$I_{CC\_180µA}$	CC1/2 pull up current	CSRC_I = 01b	165.6	180	194.4	µA
$I_{CC\_330µA}$	CC1/2 pull up current	CSRC_I = 10b	303.6	330	356.4	µA
R_{CC_open}	CC1/2 open impedance	CC1/2 in disable status	126			kΩ
$V_{CC\_0P2\_th\_src}$	CC1/2 0.2V comparison threshold	CC1/2 as source	0.15	0.2	0.25	V
$V_{CC\_0P4\_th\_src}$	CC1/2 0.4V comparison threshold	CC1/2 as source	0.35	0.4	0.45	V
$V_{CC\_0P66\_th\_src}$	CC1/2 0.66V comparison threshold	CC1/2 as source	0.61	0.66	0.7	V
$V_{CC\_0P8\_th\_src}$	CC1/2 0.8V comparison threshold	CC1/2 as source	0.75	0.8	0.85	V
$V_{CC\_1P23\_th\_src}$	CC1/2 1.23V comparison threshold	CC1/2 as source	1.18	1.23	1.28	V
$V_{CC\_1P6\_th\_src}$	CC1/2 1.6V comparison threshold	CC1/2 as source	1.5	1.6	1.65	V
$V_{CC\_2P6\_th\_src}$	CC1/2 2.6V comparison threshold	CC1/2 as source	2.45	2.6	2.75	V
$V_{TH\_CCOVP\_RISING}$	CCx OVP detection	CCOVP rising threshold		7.2		V
$V_{TH\_CCOVP\_FALLING}$	CCx OVP release	CCOVP falling threshold		7.0		V
Z_{Driver}	PD data Tx output impedance		33		75	Ω

V_{Swing}	High level voltage for CC PD data		1.05	1.125	1.2	V
VCONN SWITCH						
V_{VCONN}	VCONN input voltage		3		5.5	V
R_{VCONN}	VCONN switch on resistance	LV ≥ 3.3V			40	Ω
I_{VCONN}	VCONN current capability	VBUS_PWR = 5V		50		mA
I_{VCONN_OCP}	VCONN over current	Rising threshold		70		mA
DPDM PROTOCOL INTERFACES						
R_{SHORT}	DP DM short resistance	VBUS_PWR = 5V ~ 21V			40	Ω
$V_{3.3V}$	DPDM 3.3V buffer output voltage	VBUS_PWR = 5V ~ 21V	3.2	3.3	3.4	V
$V_{2.7V}$	DPDM 2.7V buffer output voltage	VBUS_PWR = 5V ~ 21V	2.6	2.7	2.8	V
$V_{1.96V}$	DPDM 1.96V buffer output voltage	VBUS_PWR = 5V ~ 21V	1.9	2	2.1	V
V_{TH_3V}	VTH3V comparator threshold at DPDM pin	VBUS_PWR = 5V ~ 21V	2.9	3	3.1	V
$V_{TH\_2.2V}$	VTH2.2V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	2.1	2.2	2.3	V
$V_{TH\_1.35V}$	VTH1.35V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	1.25	1.35	1.45	V
$V_{TH\_0.425V}$	VTH0.425V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	0.35	0.425	0.5	V
$V_{TH\_0.325V}$	VTH0.325V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	0.25	0.325	0.4	V
R_{OUT_30k}	Output resistance of DP or DM buffer		24	30	36	kΩ
I_{OUT_0P6V}	0.6V current capability, sink/BC1.2, DP/DM		250			μA
R_{DP/DM_DWN}	DP/DM pull down resistance	source/HVDCP, DM	16	20	24	kΩ
R_{DP/DM_LKG}	DP/DM leakage		300	500	800	kΩ
V_{DATA_HIGH}	DP/DM data output high voltage	Slave data output high, VBUS ≥ 3.3V, data_high_sel = 0	3	3.3	3.6	V
		Slave data output high, VBUS ≥ 3.3V, data_high_sel = 1	1.6	1.8	2.0	V
V_{DATA_LOW}	DP/DM data ouput low voltage	Slave data output low			0.2	V
$I_{OH\_DM\_3P3V}$	3.3V current capability, DM		5			mA
V_{IH_TH}	DPDM input data rising threshold	dpdm_in_refh_sel = 000b	0.7	0.8	0.86	V
		dpdm_in_refh_sel = 001b	1.1	1.2	1.3	V
		dpdm_in_refh_sel = 010b	1.3	1.4	1.5	V
		dpdm_in_refh_sel = 011b	1.7	1.8	1.9	V

		dpdm_in_refh_sel = 100b	1.8	1.9	2.0	V
		dpdm_in_refh_sel = 101b	2.0	2.1	2.2	V
		dpdm_in_refh_sel = 110b	2.2	2.3	2.4	V
		dpdm_in_refh_sel = 111b	2.4	2.5	2.6	V
V_{IL_TH}	DPDM input data falling threshold	dpdm_in_refl_sel = 000b	0.5	0.6	0.7	V
		dpdm_in_refl_sel = 001b	0.9	1	1.1	V
		dpdm_in_refl_sel = 010b	1	1.1	1.2	V
		dpdm_in_refl_sel = 011b	1.4	1.5	1.6	V
		dpdm_in_refl_sel = 100b	1.7	1.8	1.9	V
		dpdm_in_refl_sel = 101b	1.8	1.9	2.0	V
		dpdm_in_refl_sel = 110b	2.1	2.2	2.3	V
		dpdm_in_refl_sel = 111b	2.2	2.3	2.4	V
V_{TH_DPDMOV}	Source/DPDM OVP detection	DPDMOVP rising threshold	4.6	4.75	4.9	V
t_{DPDM_OVP}	DPDM over-voltage deglitch time	dpdm_ovp_dgl_sel = 0		4		µs
		dpdm_ovp_dgl_sel = 1		40		µs
t_{DATA_RISING}	Data output from low to high			0.3	1	µs
$t_{DATA\_FALLING}$	Data output from high to low			0.3	1	µs
t_{UI}	Unit interval time		144	160	176	µs
t_{PING_ST}	Adapter transmit slave ping duration time		2304	2560	2816	µs
t_{PING_SR}	Adapter receive master ping duration		2304	2560	2816	µs
t_{PSR}/t_{PST}	Ping received and transmit ratio		99	100	101	%
t_{AD}	Terminal attach deglitch		450	500	550	µs
t_{DD}	Terminal detach deglitch	dp_to_set = 00b	0.475	0.5	0.525	ms
		dp_to_set = 01b	0.95	1	1.05	ms
		dp_to_set = 10b	1.9	2	2.1	ms
		dp_to_set = 11b	3.8	4	4.2	ms
PDO SETTING						
V_{PDO_OPEN}	PDO1/PDO2 open voltage			VDD5V		V
I_{NTC}	PDO1/PDO2 bias current	Register programable	94	100	106	µA
		Register programable	18.8	20	21.2	
		Register programable		4	4.3	
SYSTEM CLOCK						
f_{HF_OSC}	High frequence OSC		22.8	24	25.2	MHz
f_{LF_OSC}	Low frequence OSC		475	500	525	kHz
GPIO PINS						

V_{IH_GPIO}	Input voltage high threshold	VBUS_PWR = 3.3V ~ 21V, measured as VIO	0.7	V
V_{IL_GPIO}	Input voltage low threshold	VBUS_PWR = 3.3V ~ 21V, measured as VIO	0.3	V
V_{OH_GPIO}	Output high voltage	VBUS_PWR = 6V, apply 4mA sink current from IO pin to GND externally	4.5	V
V_{OL_GPIO}	Output low voltage	VBUS_PWR = 6V, apply 10mA source current from VDD_5V to IO pin externally	0.5	V
V_{PU}	Pull up resistor value at GPIO pin	VBUS_PWR = 3.3V ~ 21V	5.1	kΩ
V_{PD}	Pull down resistor value at GPIO pin	VBUS_PWR = 3.3V ~ 21V	5.1	kΩ
THERMAL SHUTDOWN				
T_{TH}	Thermal shutdown threshold (LDO), SC2021A will reset when junction temperature is over T_{TH}	T_{TH} rising	160 180	℃
T_{TH_HYS}	Over temperature hysteresis	T_J falling below T_{TH} - T_{TH_HYS}, SC2021A will restart.	15	℃

(1). It is recommended to set VDAC code at least 60 at 3.2V on VBUS.

8 Detailed Description

8.1 Power Supply

SC2021A contains an internal high-voltage LDO which supports wide input range. VBUS_PWR is the power supply input pin of internal LDO. It converts voltage on VBUS_PWR to 5V and supplies internal modules.

For applications, VBUS_MON should be connected to the VBUS on USB port, and VBUS_PWR should be connected to internal VBUS node. It is recommended to place a 1μF ceramic capacitor close to the VDD5V pin.

8.2 NMOS Gate Driver

The Type-C and USB PD specifications require the VBUS isolation implementation for the Type-C port. SC2021A provides NMOS gate driver to control the isolation MOSFET between the internal VBUS node and the Type-C port. The gate driver is controlled by register bit. The voltage VGS is clamp to 7V. The IC provides 4 different pull-up capabilities from 20kΩ to 200kΩ so to suit different MOSFETs.

8.3 VBUS Discharging Paths

The IC integrates VBUS discharging paths from VBUS_MON VBUS_PWR and VBUS_A pins to ground respectively. These paths help drain the residual charge on the bulk capacitors to meet the application requirements. The typical equivalent impedance of discharge path on VBUS_MON pin and VBUS_A pin are 1kΩ. Discharging path on VBUS_PWR pin is a constant current from 45mA to 150mA, which can be configured by registers. These discharge paths are activated at detachment or a lower VBUS voltage transition occurring. All discharging paths can be controlled by firmware.

8.4 ADC

In the Type-C, USB PD or other quick charge applications, it is necessary to monitor the VBUS voltage and current. The SC2021A integrates a 10-bit Successive Approximation Analog to Digital Converter (SAR ADC) with a reference voltage of 2.253V at a sampling rate from 5kHz to 50kHz.

The ADC supports 10-channel input as below. For VBUS_MON VBUS_PWR and VBUSA, an internal ratio of 1/10 is built in. The ratio of DPDM and VDD5V channel is 1/4.

The Internal Temperature Sense (ITS) unit converts the temperature to voltage. Users can get the die temperature by sampling the channel. The ratio of voltage to temperature is 2.819mV/℃ and the output of ITS is 733.94mV at the temperature of 27℃.

Table 1. ADC input channel

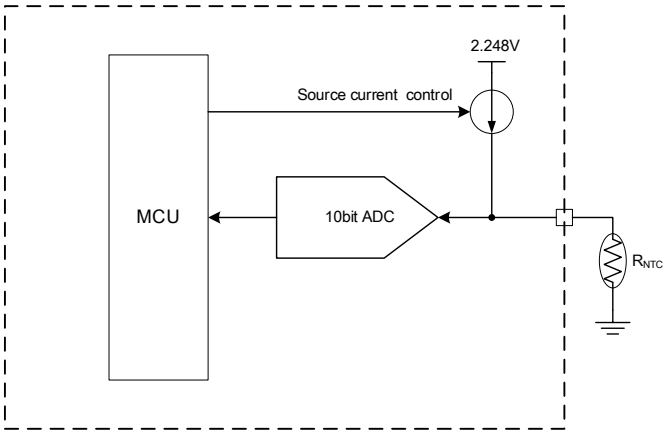
ADC_CH_SEL[3:0]	Input Signal	Note
0000	1/10 x VBUS_PWR	With 1/10 internal divider
0001	1/10 x VBUS_MON	With 1/10 internal divider
0010	VRSNS × 40 or 20	The gain of current sense amplifier can be set as 40 or 20
0010	1/4 x DPx or DMx	With 1/4 internal divider
0100	1/4 x VDD5V	With 1/4 internal divider
0101	AD2	
0110	AD1	
0111	AD0	
1000	ITS	Internal temperature sense
1001	1/10 x VBUSA	With 1/10 internal divider

8.5 PDO Setting

SC2021A provides two ports to support external PDO setting. The PDO pin can source a bias current and can be configured as input of ADC channel. SC2021A broadcasts different source capabilities through CC or DPDM by detecting the resistors connected to PDO pins.

As shown in the figure, the PDO pins can be used for temperature detecting. Each of NTC pins source current on the R_{NTC}, and the voltage can be sampled by 10-bit ADC. Source current can be configured as 100μA, 20μA or 4μA.

The over-temperature protection will be triggered if the voltage is below an over-temperature protection threshold for a programmed time delay.



8.6 CV CC Control Loop for ACDC

SC2021A contains 2 DACs and 2 error amplifiers for OPTO pin to regulate output voltage and current. For voltage regulation, VDAC is a 10-bit DAC with internal 2.048V reference voltage. SC2021A supports at least 20mV per step for VBUS output voltage regulation. The adjust time ranges from 20 μs to 250 μs which can be set by firmware.

VBUS output regulation should be as the following equation.

$$V_{REG} = 2 + VDAC\ code * 0.020$$

For example, if VDAC code = 150, the output voltage V_{REG} = 5V.

SC2021A integrates a high side current sense amplifier for constant current regulation and output current sampling. The gain of the amplifier can be configured as 40 or 20. For 3mohm application, SC2021A supports up to 8A constant current regulation.

The IDAC is 10-bit with 1.2V reference. The regulation current (I_{REG}) is decided by IDAC code, sense resistance (R_{SNS}) and the gain of current sense amplifier (G_{SNS}). The relationship between these parameters should be as follows.

$$I_{REG} = \frac{IDAC\ code \times 1.2}{(2^{10} \times R_{SNS} \times G_{SNS})}$$

For example, if R_{SNS} = 5mΩ, G_{SNS} = 40, IDAC code = 512, I_{REG} = 3A.

8.7 CV CC Control Loop for DCDC

Generally, DCDC output voltage and current is controlled through the FB pin, so SC2021A integrates another set of voltage and current regulation for DCDC application.

SC2021A can source current or sink current to DCDC FB, which is equivalent to changing the voltage divider ratio of the feedback node. For voltage regulation, FBVDAC outputs voltage from 0 to 1023 mV. Each step corresponds to 1mV. Current magnitude is decided by the following equation, and direction is set by register.

$$I_{FB} = \frac{V_{FBVDAC}}{R_{FBS}}$$

The relationship between V_{FBDAC} and DCDC output voltage is as follows.

$$V_{OUT} = \left(1 + \frac{R_{UP}}{R_{DWN}}\right) V_{REF} - \frac{V_{FBVDAC} \cdot R_{UP}}{R_{FBS}} \text{ (FB source current)}$$

$$V_{OUT} = \left(1 + \frac{R_{UP}}{R_{DWN}}\right) V_{REF} + \frac{V_{FBVDAC} \cdot R_{UP}}{R_{FBS}} \text{ (FB sink current)}$$

V_{REF} is the reference voltage of power IC. R_{UP} and R_{DWN} are the resistor divider. R_{FBS} is the resistance between FBS pin and ground.

For current regulation, it is the same to ACDC application except the reference voltage. It is decided by the following equation.

$$I_{FBREG} = \frac{IDAC\ code \times 2.248}{(2^{10} \times R_{SNS} \times G_{SNS})}$$

For example, if R_{SNS} = 5mΩ, G_{SNS} = 40, IDAC code = 512, I_{FBREG} = 5.62A.

8.8 DPDM Interface

The SC2021A contains 2 DPDM interfaces which can be configured as discharging out port (provider). The DPDM interfaces are available for USB-A port applications or Type-C port applications. It supports Apple-2.4A, BC1.2 DCP, HVDCP, FCP, SCP, VOOC and other proprietary fast charging protocols.

All of the DPDM pins can be configured flexible for different applications. SC2021A supports Apple-2.4A mode, which broadcasts 2.7V voltage on both DP and DM pins with 30kohm output impendence. If 2.4A mode advertisement on DPDM is enabled, it is recommended that VBUS should be able to supply at least 2.4A of current.

SC2021A can be also configured as a dedicated charging port (DCP), which complies with the BC1.2 specification. When DCP mode is enabled, SC2021A shorts DP and DM pin through a 20ohm resistor.

SC2021A supports HVDCP mode for some high voltage protocols. Under HVDCP mode, DPx and DMx can check the voltage by internal comparators or detect some proprietary fast charging protocols such as SCP, UART and I2C.

8.9 CC Interface

The IC can be configured as source only. It presents Rp on CC1 and CC2. CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable. Once an attachment is detected, the IC will apply VBUS voltage and broadcast source capabilities.

Current source presented on CC can be configured to 330μA, 180μA and 80μA. Each of the CC pins contains comparators to decide CC_RD and CC_RA attachment.

8.9.1 VCONN Switch

SC2021A features a more than 50mA VCONN power with a fixed Overcurrent Protection (OCP) of 70mA.

The IC supports electronically marked cables assembly for more than 3A power delivery. By default, passive cables support up to 3A. The IC can check the cable types through internal CC comparators. If an e-marker cable is detected, the IC supplies the cable with VCONN and communicates with it to check the cable current ratings. As a consequence, source power supply advertises any PDO if cable is identified as able to sustain such current. Refer to PD specification, the IC supports up to 5A power delivery application.

When VCONN switch is turned on, SC2021A will continuously monitor current on CC pin. If VCONN output current is above 70mA, VCONN over-current flag will be set, and VCONN switch can be turned off by firmware. SC2021A supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

When VCONN switch is turned on, the IC will continuously monitor current on CC pin. VCONN over-current flag will be set if VCONN output current is above 70mA. Once VCONN OCP is triggered, VCONN switch can be turned off by firmware. The IC supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

8.10 USB PD Protocol

The IC provides USB PD physical layer for PD protocols communication. The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. Once the insertion direction of Type-C port is detected by CC comparator, the IC can select either CC1 or CC2 channels to send and receive PD packets. All processes of PD communication are controlled by firmware.

8.11 Protections

8.11.1 OVP, UVP and SCP

The IC monitors the VBUS voltage in real time. Once the voltage exceeds the OVP threshold for a programmed time, the flag is set and an interrupt is generated automatically. It also monitors VBUS voltage for under-voltage protection (UVP). Once VBUS voltage drops below UVP threshold for a programmed time, the UVP flag is set and an interrupt is generated. Once voltage on VBUS drops below 3.2V, Short-Circuit Protection (SCP) will be triggered. An interrupt will be generated and the SCP flag will be set.

The OVP threshold, UVP threshold and the detection deglitch time can be configured through registers. The OVP threshold can be configured as 110%, 115% and 120% of the setting voltage, while UVP threshold can be configured as 75%, 85% and 95%. The deglitch time can be configured as 4 µs or 40 µs.

8.11.2 Protection for DPDM

The IC supports over-voltage protection of the DP/DM pin. Once it detects any of the DP and DM voltage exceeding 4.75V, the IC will report the over-voltage status and generate an interrupt.

8.11.3 Protection for CC

SC2021A continuously monitors CC voltage. Once CC over-voltage detected, SC2021A will launch CC Over-Voltage Protection (CC OVP). The CCOVP flag will be set if the voltage on CC1 or CC2 is over 7.2V and will be clear after voltage falls below 7V. The OVP interrupt will be triggered if interrupt enable control bit is set.

If each of the protections including OVP, UVP, SCP is detected, SC2021A can drive isolation MOS off by register setting.

8.12 MCU Controller

8.12.1 Clock

The SC2021A integrates a 24MHz high frequency clock and a 500kHz low frequency clock. Under normal working condition, high frequency and low frequency clocks work simultaneously. When in sleep mode, only the 500kHz clock works to reduce the power consumption.

8.12.2 Modes

The SC2021A supports three operating modes: active mode, standby mode and sleep mode. In active mode, each function module operates normally. In standby mode, MCU stops, each module can be turned on and MCU restarts once any of the interrupts is triggered. In sleep mode, only the 500kHz low frequency clock works, and all other functions are turned off. The quiescent current can be as low as 200 µA in sleep mode.

After entering sleep mode, the system can be awakened by interruptions, including GPIO interrupts, DPDM interrupts, watchdog interrupts, and the timer interrupts with the 500kHz clock source.

8.12.3 GPIO

GPIO has input/output direction settings, internal pull-up/pull-down resistor settings, and interrupt edge settings.

8.12.4 Interrupts

The IC supports various interrupts, including Timer0 interrupt, Timer1 interrupt, ADC interrupt, I2C interrupts, DPDM interrupts, analog interrupts, WDT interrupt, IOx interrupt.

8.12.5 Timer

The SC2021A integrates two general timers. The clock source can be configured as 24MHz high frequency oscillator or 500kHz low frequency oscillator.

The timer0 is a count-down counter. Counting cycle and clock can be configured by registers. Overflow flag will be set and interrupt will be generated once timer0 counts to the end of cycle.

Timer1 is a count-up counter. The counting cycle and clock can be configured by registers. Overflow flag will be set and an interrupt will be generated once timer1 counts to CCR0 register value. In addition, timer1 could be configured as a PWM output. By default, when timer1 counter counts to CCR0, TMR1 output low. When timer1 counts to CCR1, TM2 output high. The period and duty of PWM output is decided by the value of CCR0 and CCR1.

8.12.6 UART

UART can support Tx function and Rx function. The baud rate can be set from 9600 bit/s to 921600 bit/s.

8.12.7 I2C

The SC2021A contains two I2C interface. One is controlled by hardware and the other is software controlled. For the software controlled I2C, it can be configured as a master interface or a slave interface. If the I2C is a slave one, the slave address is defined by firmware.

For the hardware I2C interface, SC2021A contains 36Byte register for data exchange, which can be accessed by external application processor and internal firmware. The read and write permissions are shown in the following table.

Addr.	I2C		Firmware	
	Write	Read	Write	Read
0x00-0x0F	Available	Available	NA	Available
0x10-0x1F	NA	Available	Available	Available
0x20-0x23	Available	Available	Available	Available

8.12.8 Watchdog

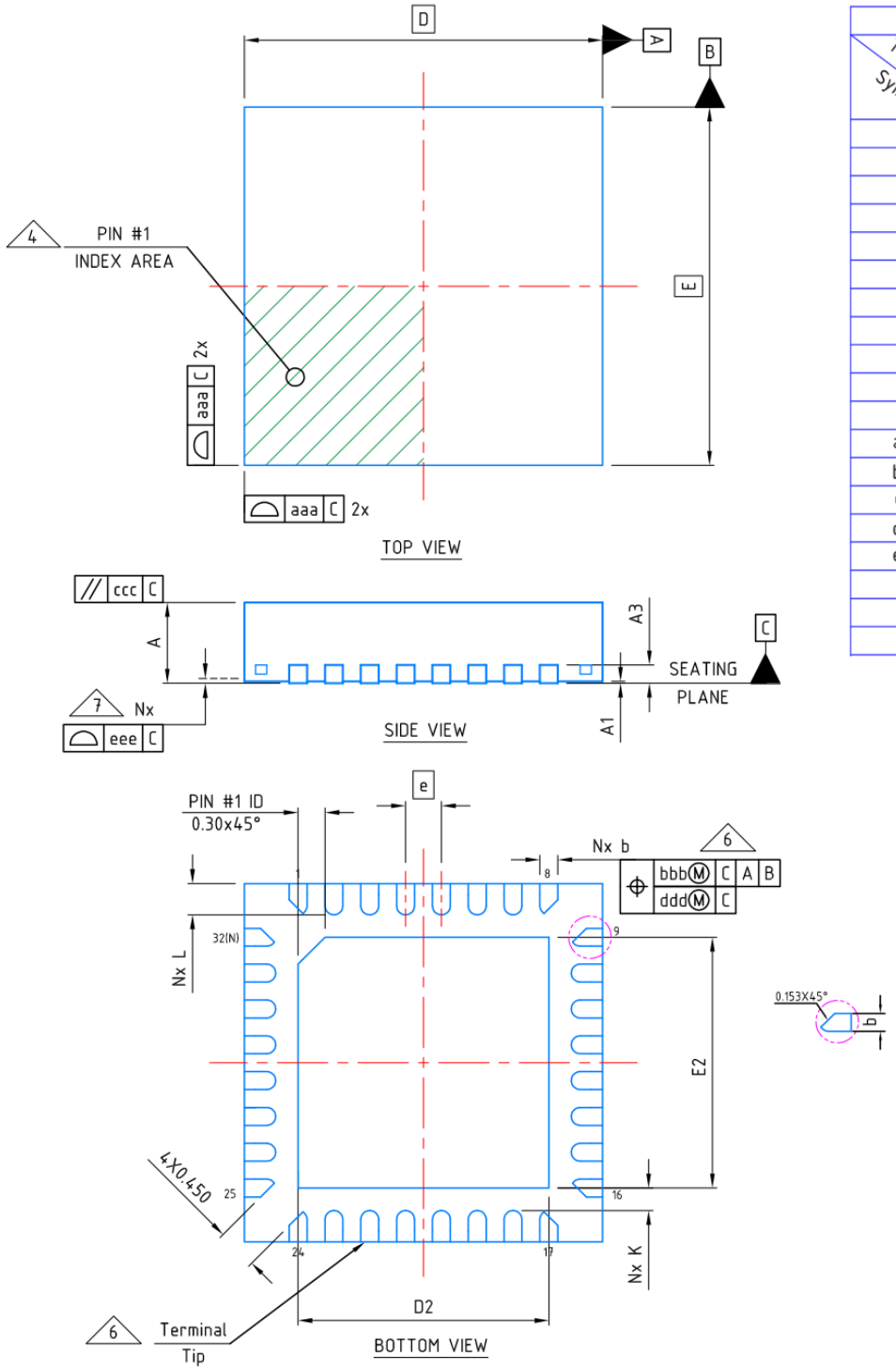
The watchdog is a 16-bit counter with 1000Hz clock source (divided from 500kHz clock). Once the watchdog is enabled, the watchdog counter starts with the value of zero and counts up. The control register WDT_CTRL can be used to select whether an interrupt or reset signal, or both occurs when the counter overflows (counting to WDT_INIT).

8.12.9 Programming

The SC2021A can be programmed through I2C interface, CC and DPDM.

PACKAGE

QFN-32 0404 x 0.75



Dimension Table			
Thickness / Symbol	W		
	MINIMUM	NOMINAL	MAXIMUM
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	---	0.20 ref	---
b	0.15	0.20	0.25
D	3.95	4.00	4.05
E	3.95	4.00	4.05
e	---	0.40 BSC	---
D2	2.70	2.80	2.9
E2	2.70	2.80	2.90
K	0.20	---	---
L	0.25	0.35	0.45
aaa	0.05		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	32		
ND	8		
NE	8		

Board Layout Example