15W Wireless Power Transmitter SOC

1 Descriptions

The SC9608 is a highly integrated wireless power transmitter SOC solution that contains both digital microcontroller and analog front end (AFE). The microcontroller includes a high performance 32-bit digital core, rich memory and peripherals. The AFE includes a full-bridge power MOSFETs, current sense amplifier, communication demodulator, linear regulator and protection circuit. The SC9608 supports various type of transmitter include both Extended Power Profile (EPP) and Baseline Power Profile (BPP) defined in WPC V1.2.4.

The SC9608 integrates CC&DP/DM interface. To implement an EPP transmitter system, the SC9608 can request a high voltage from the adapter through CC1/CC2 or DP/DM interface. The SC9608 supports foreign object detection (FOD) by continuously monitoring the input voltage and input DC current. Besides, the SC9608 also supports input under-voltage lockout (UVLO), over-current protection (OCP) and over-temperature protection (OTP). These protections further enhance the reliability of the total wireless power transmitter system.

The SC9608 is available in a compact 4x4 mm FCQFN package.

2 Features

- 4.0V to 14.0V AVIN input voltage range
- 2.0V to 14.0V PVIN input voltage range
- Support up to 15W output power
- Integrated voltage and current demodulation
- Integrated low R_{DSON} power FETs
- Integrated FET driver and bootstrap circuit
- Integrated accurate current sense for FOD
- Support DP/DM fast charging interface
- Support USB Power Delivery
- UVLO/OVP/OCP/OTP
- 4mm x 4mm FCQFN package

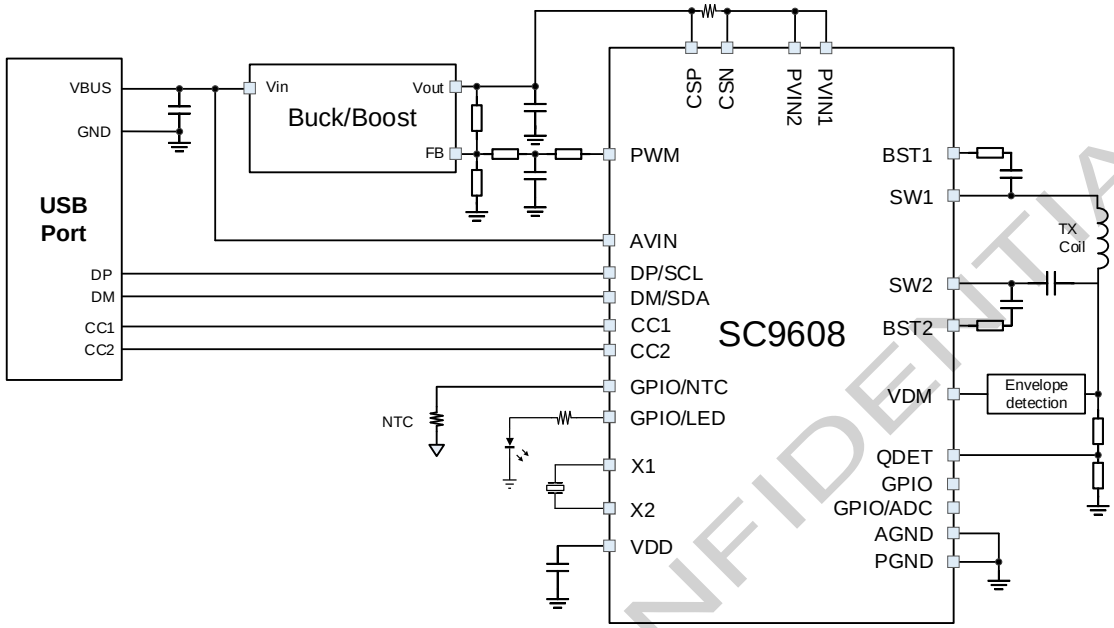
3 Applications

- WPC Compliant Wireless Power Transmitter
- Proprietary Wireless Chargers and Transmitter

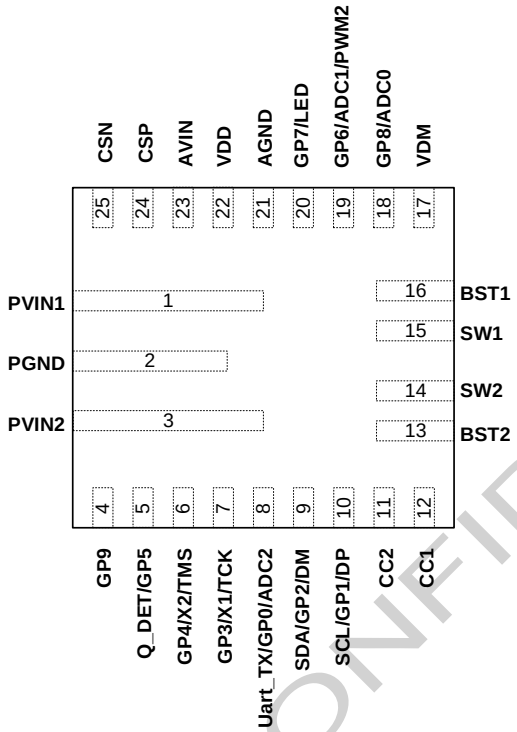
4 Device Information

Part Number	Package	Dimension
SC9608QFER	FCQFN25	4mm x 4mm x0.75mm

5 Typical Application Circuit



6 Terminal Configuration and Functions



Pin Map (Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	PVIN1	PWR	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
2	PGND	PWR	Power ground.
3	PVIN2	PWR	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
4	GP9	I/O	GPIO
5	Q_DET/GP5	I/O	Quality factor detection input/ GPIO
6	GP4/X2/TMS	I/O	GPIO/ external crystal output/ TMS
7	GP3/X1/TCK	I/O	GPIO/ external crystal input/ TCK
8	UART/GP0/ADC2	I/O	UART/GPIO/ADC0
9	SDA/GP2/DM	I/O	I2C Serial data line/ GPIO/ DM pin for type A USB port interface
10	SCL/GP1/DP	I/O	I2C Serial clock line/ GPIO/ DP pin for type A USB port interface

11	CC2	I/O	CC2 line of USB Type-C port
12	CC1	I/O	CC1 line of USB Type-C port
13	BST2	I/O	Positive supply rail for high-side gate driver. Connect a 0.1 µF capacitor and a 4.7Ω resister between BST2 and SW2
14	SW2	PWR	Switch node of the half-bridge MOSFET.
15	SW1	PWR	Switch node of the half-bridge MOSFET.
16	BST1	I/O	Positive supply rail for high-side gate driver. Connect a 0.1 µF capacitor and a 4.7Ω resister between BST1 and SW1
17	VDM	I	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation
18	GP8/ADC0	I/O	GPIO/ ADC
19	GP6/ADC1/PWM	I/O	GPIO/ ADC/ PWM generator output pin
20	GP7/LED	I/O	GPIO/ LED driver
21	AGND	PWR	Analog Ground
22	VDD	O	Output of internal regulator to provide 5.0V power supply to internal gate drivers and control circuits. Connect a 1 µF ceramic capacitor from VDD to AGND pin.
23	AVIN	PWR	Input voltage for internal LDO converter, Bypass with a 4.7 µF ceramic capacitor to GND
24	CSP	I	Input current sense amplifier positive input
25	CSN	I	Input current sense amplifier negative input

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	PVIN1, PVIN2, SW1, SW2, AVIN, CC1, CC2, CSP, CSN	-0.3	16	V
	BST1, BST2	-0.3	21	V
	Others	-0.3	5.5	V
	QDET(100ns transient)	-1.5	6	V
	VDM(1ms transient)	-0.3	7.5	V
Temperature Range	Operating Junction, T_J	-40	125	°C
	Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2)	-2000	2000	V
	Charged device model (CDM) ESD stress voltage (3)	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{PVIN1}, V_{PVIN2}	Input voltage range	2		14	V
V_{AVIN}	Input voltage range for internal LDO convertor	4		14	V
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 Ceramic Capacitor		22		µF
C_{BST1}, C_{BST2}	BST1-SW1, BST2-SW2 Ceramic Capacitor		0.1		µF
C_{AVIN}, C_{VDD}	AVIN, VDD Ceramic Capacitor		2.2		µF
T_A	Operating ambient temperature	0		85	°C
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL RESISTANCE(1)		QFN-25 (4mm x 4mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	44	°C/W
Θ_{JC}	Junction to case resistance	11	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristic

T_J= 25°C, V_{AVIN} =V_{PVIN1} = V_{PVIN2} = 9.0V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{AVIN}	Operating voltage		4		14	V
V_{AVIN_UVLO}	Under voltage lockout threshold	Rising edge	3.65	3.8	3.95	V
		Hysteresis		200		mV
I_Q	Quiescent current into AVIN	Normal mode, no switching		5	10	mA
I_{LP}(1)	Low power current into AVIN	Low power mode		140		μA
VOLTAGE REGULATOR (VDD)						
V_{DD}	VDD output voltage	V_{AVIN} = 9.0V, I_{VDD} =10mA	4.75	5	5.25	V
I_{VDD_LIM}	VDD current limit	V_{DD} = 5.0V		50		mA
V_{DROP}		V_{AVIN} = 4V, I_{VDD} =10mA		200		mV
PROTECTION						
V_{AVIN_DPM}	Dynamic power management	P_AVDPM_CFG[1:0]=0		4.2		V
		P_AVDPM_CFG[1:0]=1		4.4		V
		P_AVDPM_CFG[1:0]=2		4.6		V
		P_AVDPM_CFG[1:0]=3		4.8		V
V_{DPM_HYS}	AVIN DPM Hysteresis	P_AVDPM_HYS=0		0.2		V
		P_AVDPM_HYS=1		0.4		V
V_{AVIN_DROP}	AVIN drop protection	P_AVDRP_CFG=0		8.5		V
		P_AVDRP_CFG=1		11.5		V
V_{DROP_HYS}	AVIN drop Hysteresis			0.25V		V
V_{AVIN_OV}	AVIN over voltage warning	P_AVOV_CFG[1:0]=0		6		V
		P_AVOV_CFG[1:0]=1		10		V
		P_AVOV_CFG[1:0]=2		13		V
		P_AVOV_CFG[1:0]=3		15		V
$V_{AVIN\_OV\_HYS}$	AVIN over voltage warning hysteresis			1		V
V_{PVIN_OV}	PVIN over voltage warning			15		V
$V_{PVIN\_OV\_HYS}$	PVIN over voltage warning hysteresis			1		V

I_{COIL_P}(1)	Coil peak current OCP	HSOC_SET[2:0]=0	6	A
		HSOC_SET[2:0]=1	7	A
		HSOC_SET[2:0]=2	8	A
		HSOC_SET[2:0]=3	9	A
		HSOC_SET[2:0]=4	10	A
		HSOC_SET[2:0]=5	11	A
		HSOC_SET[2:0]=6	12	A
		HSOC_SET[2:0]=7	13	A
$I_{COIL\_P\_CNT}$(1)	Coil peak current OCP deglitch count	HSOC_CNT_SEL=0	4	
		HSOC_CNT_SEL=1	8	
t_hiccup(1)	hiccup time after OCP		10	ms
POWER SWITCH				
$R_{DS(on)}$	Q1/Q2/Q3/Q4 $R_{DS(on)}$	V_{DD} = 5.0V	22	mΩ
T_{DEAD}(1)	dead time	DEAD_TIME[2:0]=0	15	ns
		DEAD_TIME [2:0]=1	25	ns
		DEAD_TIME [2:0]=2	35	ns
		DEAD_TIME [2:0]=3	45	ns
		DEAD_TIME [2:0]=4	55	ns
		DEAD_TIME [2:0]=5	65	ns
		DEAD_TIME [2:0]=6	75	ns
		DEAD_TIME [2:0]=7	85	ns
Voltage Demodulation				
V_{DM_HYS}	VDM input hysteresis voltage	DM0_HYS[2:0]=0	5	mV
		DM0_HYS[2:0]=1	10	mV
		DM0_HYS[2:0]=2	20	mV
		DM0_HYS[2:0]=3	30	mV
		DM0_HYS[2:0]=4	40	mV
		DM0_HYS[2:0]=5	60	mV
		DM0_HYS[2:0]=6	80	mV
		DM0_HYS[2:0]=7	100	mV
Current Demodulation				
I_{DM_HYS}	IDM input hysteresis voltage	DM1_HYS[2:0]=0	5	mV
		DM1_HYS[2:0]=1	10	mV
		DM1_HYS[2:0]=2	20	mV
		DM1_HYS[2:0]=3	30	mV
		DM1_HYS[2:0]=4	40	mV
		DM1_HYS[2:0]=5	60	mV
		DM1_HYS[2:0]=6	80	mV

		DM1_HYS[2:0]=7	100	mV
Q_DET				
V_{Q_BIAS}	Bias voltage on SW1		2.5	V
$V_{Q\_TH\_HIGH}$(1)	Q detection comparator High TH		200	mV
$V_{Q\_TH\_LOW}$(1)	Q detection comparator Low TH		100	mV
GPIO				
V_{IH}	Input logic high		1.2	V
V_{IL}	Input logic low		0.4	V
V_{OH}	Output logic high	source 5mA	0.9* V_{DD}	V
V_{OL}	Output logic low	sink 5mA	0.1* V_{DD}	V
R_{PU}	Pull up resistor value at GPIO pin		5.5	kΩ
R_{PD}	Pull down resistor value at GPIO pin		5.5	kΩ
I_{LKG_GPIO}	Input leakage current	V_{IN}=5V	1	μA
ADC				
N	Resolution Guarantee 9 bit		10	bit
F_{SAMPLE}	PVIN & AVIN & IIN channels		5	kSa/s
F_{SAMPLE}	other channels		20	kSa/s
Channel	Number of channels		7	
V_{FS}	Full scale voltage		2.048	V
CURRENT SENSE				
I_{IN}	input current range		0 2.5	A
Gain	R_{SENSE}=10mohm	DCSNS_SEL20X=0	0.7	V/A
	R_{SENSE}=20mohm	DCSNS_SEL20X=1	0.7	V/A
	Gain error	I_{SENSE}>0.5A	-2% 2%	
V_{OO}	Sampling output offset voltage	V_{CSP}=V_{CSN}	0.25	V
VOLTAGE SENSE				
$V_{PVINSENSE}$	PVIN sense range		0.5 15.5	V
	sense accuracy	V_{PVIN}>3.5V	-0.5 0.5	%
$V_{AVINSENSE}$	AVIN sense range		3.5 15.5	V
	sense accuracy		-0.5 0.5	%
TDIE SENSOR				
T_{DIE}(1)	TDIE sense range		-40 150	°C
	sense accuracy		-5 5	°C
FPWM				
F_{SW}	PWM switching frequency		105 210	kHz
Duty	PWM duty cycle		0% 100%	

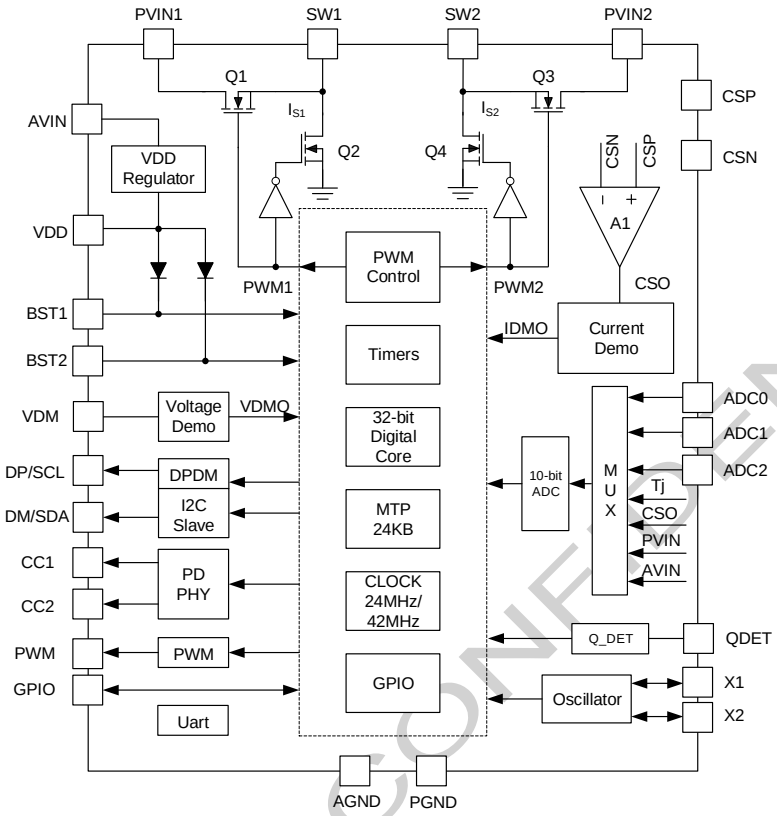
Phase	PWM phase ratio		0	180	°
External PWM					
F_{PWM2}	PWM frequency		24		kHz
D_{PWM2}	PWM duty range		0	100	%
	Resolution		0.1		%
DP/DM					
R_{DM_DWN}	DP/DM pull down resistance		20		kΩ
R_{DP_LKG}	DP pin leakage resistance		500		kΩ
V_{DPDM_OVP}	DP/DM OVP threshold		4.7		V
CC					
R_{PD_CC}	CC1/2 pull down resistor	$V_{CC1/2}$ = 0V to 2.5V	5.1		kΩ
R_{CC_OPEN}	CC1/2 open impedance	CC1/2 in disable status or error status	126		kΩ
V_{CC_OVP}	CC1/2 OVP threshold		6.4		V
External Crystal					
F_{XTAL}			24	48	MHz
Start time(1)			2		ms
SDA,SCL					
V_{IH}	Input Threshold High		1.4		V
V_{IL}	Input Threshold Low			0.4	V
I_{LKG}	Input Leakage Current		-1	1	μA
V_{OL}	Sink = 3mA			0.4	V
F_{SCL}				400	kHz
T_{LOW}	Clock low		1.3		μs
T_{HIGH}	Clock high		0.6		μs
C_B	Capacitive Load for SCL and SDA		150		pF
C_I	SCL, SDA Input Capacitance		5		pF
CLOCK					
F_{SYSTEM}	System OSC frequency		24		MHz
	System OSC frequency error		-3%	3%	
F_{PWM}	Full bridge PWM clock		42		MHz
	Full bridge PWM clock error		-1%	1%	
THERMAL SHUTDOWN					
T_{SD}(1)	Thermal shutdown temperature		150		°C
T_{SD_HYS}(1)	Thermal shutdown hysteresis		20		°C
T_{WN}(1)	Thermal warning temperature	P_TSW_CFG[2:0]=0	65		°C
		P_TSW_CFG [2:0]=1	75		°C
		P_TSW_CFG [2:0]=2	85		°C

		P_TSW_CFG [2:0]=3	95	°C
		P_TSW_CFG [2:0]=4	105	°C
		P_TSW_CFG [2:0]=5	115	°C
		P_TSW_CFG [2:0]=6	125	°C
		P_TSW_CFG [2:0]=7	135	°C
T_{WN_HYS}(1)	Thermal warning hysteresis		10	°C

Notes:

(1) Guaranteed by design and characterization test.

8 Functional Block Diagram



9 Detailed Description

The SC9608 device is a highly integrated wireless power transmitter SOC solution supporting up to 15W power output.

9.1 Power Supply

The SC9608 integrates a high-voltage low-dropout (LDO) voltage regulator powered from AVIN. It feeds the internal power drivers and control circuits. The VDD pin supplies a regulated 5.0V voltage supply. Decouple this pin to power ground with a 2.2μF low ESR ceramic capacitor placed close to the IC.

The internal LDO works once AVIN is above the UVLO threshold. The load capability of VDD regulator is about 30mA. Please do not power up other load from the internal LDO.

9.2 Under-Voltage Lockout (UVLO)

The UVLO function protects the chip from operating at insufficient power supply. The chip disables all the function if AVIN voltage is lower than 3.6V (typical) and it does not start up again until input voltage is higher than 3.8V (typical).

9.3 Current Sense

To support foreign object detection (FOD), the SC9608 integrates a lossless current sense amplifier to senses the average input current. User should always monitor the voltage of ADC channel 5 to calculate the input current. Gain of the input current to the sampling output voltage is 0.7V/A.

When the input current is zero, the sampling output has an offset voltage. The offset voltage is about 0.25V.

The offset may have some variation. For accurate measurement of the input current, MCU need to calibrate the offset before power stage switching.

9.4 Full-Bridge invertor

The SC9608 integrates a high efficiency full-bridge invertor with ultra-low R_{DS} to convert the DC power signal to AC power. The drive ability of FET is adjustable bring more convenience for EMI test.

The SC9608 also integrates a PWM peripheral to control the full-bridge invertor. The PWM1 controls the internal MOSFET Q1 and Q2, and PWM2 controls the internal MOSFET Q3 and Q4 as shown in the Block Diagram. The invertor also can work in half-bridge mode by disenable PWM1 or PWM2.

There are four configuration registers for customer to configure: PWM_PERIOD [15:0], PWM_DUTY [15:0], PWM_DEADTIME [15:0] and PWM_PHASE [15:0]. For a target switching frequency F_{SW} (Hz), the PWM_PERIOD [15:0] register should be configured to PWM_CLOCK/F_{SW}. The internal 24MHz oscillator and 42MHz oscillator are alternative for PWM CLOCK. PWM_DUTY [15:0] register should always be programmed to half of the PWM_PERIOD [15:0] register.

PWM_DEADTIME [15:0] register is used for the duty cycle control of full-bridge. The formula is as follows:

Duty=50%- PWM_DEADTIME [15:0]/PWM_PERIOD [15:0]

PWM_PHASE [15:0] register is used for phase shift mode.

Phase=(PWM_PHASE [15:0]/PWM_PERIOD [15:0])*360°

For duty cycle control mode, to set 50% duty cycle, the PWM_DEADTIME [15:0] should be configure to 0. To set 10% duty cycle, the PWM_DEADTIME [15:0] should be configure to 0.4* PWM_PERIOD [15:0]. The generation theory of PWM1/2 is as below figure 1.

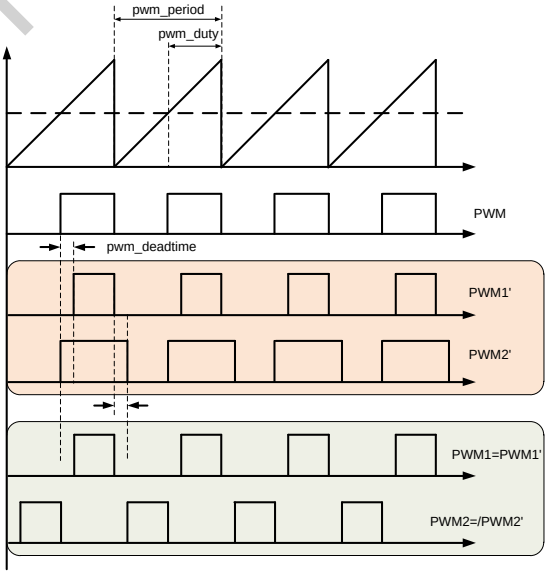


Fig1. Duty cycle control mode

For phase shift control mode, to set 30° phase shift, the PWM_PHASE [15:0] should be configure to PWM_PHASE [15:0]/12. The phase shift control method is as below figure 2.

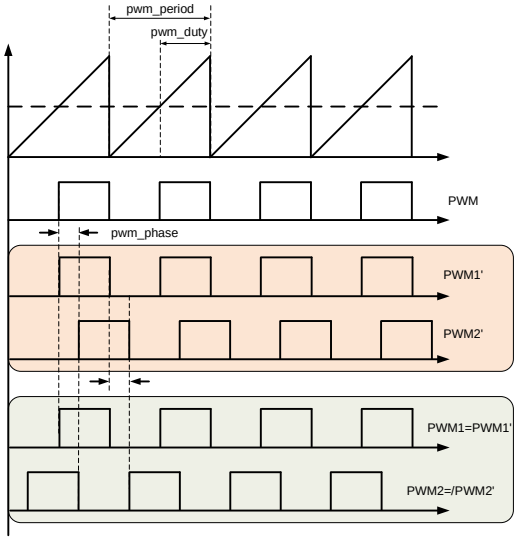


Fig2. Phase shift control mode

9.5 High-side bootstrap driver

The SC9608 integrates bootstrap driver for high-side FETs driving. Connecting a 0.1uF capacitor and a 4.7Ω resister between BST and SW pins is highly recommended for better turn-on/off performance of high-side FETs.

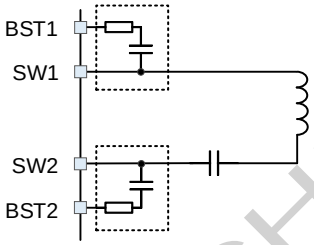


Fig3. Bootstrap driver capacitor and resistor connection

9.6 ASK Demodulation

To increase the communication reliability in any load condition, the SC9608 has integrated two demodulation schemes, one based on input average current information and the other based on coil voltage information. The ASK voltage envelope detector is implemented using a discrete solution as depicted on figure 4. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

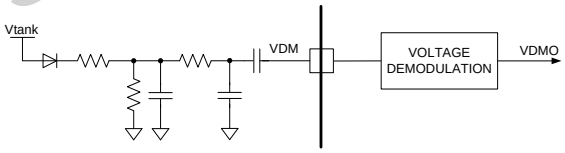


Fig4. Voltage Demodulation

The current demodulation module takes the modulation information from the internal CSO output signal indicated the average input current. The MCU can detect the demodulation results on internal VDMO and IDMO signals and then implement the packet decode. The MCU can select either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

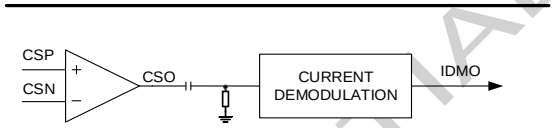


Fig5. Current Demodulation

The comparator hysteresis of voltage-mode and current-mode demodulation circuits are both adjustable to achieve better system communication performance.

9.7 ADC

The SC9608 integrates a 10-bit SAR ADC to sense the external and internal voltages. The full-scale of ADC reference voltage is 2.048V, which means 2mV/LSB.

Table1. ADC channels

Channel	Signal	Description
CH0	ADC0	External voltage sense
CH1	ADC1	External voltage sense
CH2	ADC2	External voltage sense
CH3	TDIE	Die temperature sense
CH4	CSO voltage	CSO voltage sense
CH5	PVIN voltage	PVIN voltage sense
CH6	AVIN voltage	AVIN voltage sense

9.8 Q Factor Detection

The SC9608 integrates an accurate Q factor detection circuit to implement foreign objects detection before the selection phase. The formula is as follows:

$Q=\Delta T*\pi/10/\ln 2$

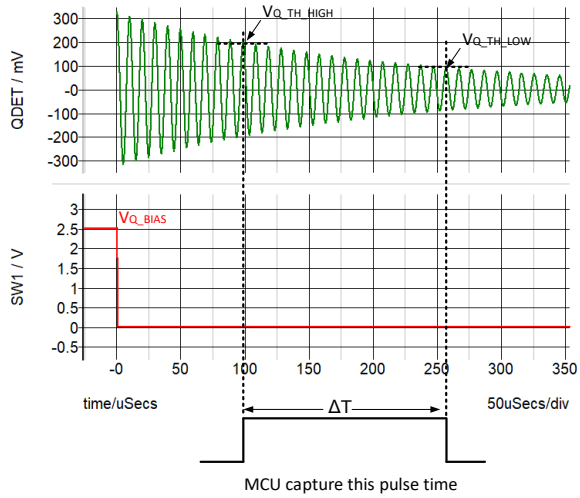


Fig6. Operation principle of Q factor detection

9.9 External PWM generator

The SC9608 integrates an external PWM generator used to adjust the DC-DC convertor output voltage. The fixed frequency of PWM is 24 kHz, and PWM duty is programmable from 0% to 100%. The adjustment resolution of PWM duty is about 0.1%.

9.10 External crystal oscillator

The SC9608 integrates a crystal driver for high precision and steady clock. This module provides more accuracy reference clock for full bridge PWM driver control. The range of crystal should be 24MHz to 48MHz.

9.11 DPDM Interface

The SC9608 integrates DPDM interface with different kind of fast charge protocols supported. The DPDM interface is available for Micro-B and Type-C port applications. It supports the mainstream fast charging protocols, such as BC1.2, DCP, HVDCP, FC, AFC and FCP etc.

9.12 CC1/2 Interface

The SC9608 integrates CC1/2 interface meeting the Type-C protocol and providing USB PD physical layer for PD protocol communication. User can easily implement the Type-C sink protocol and PD protocol through the packaged software interface.

9.13 Over-Current Protection (OCP)

The SC9608 integrates an over-current protection function which monitoring the peak current through the full-bridge and coil cycle by cycle. The device senses the current of the high-side FET and compare to the current-limit threshold during every switching cycle. When the sensed current reaches the current-limit threshold, the over-current fault counter is incremented. If the over-current fault counter reaches the setting value (DTX_HSOC_CNTSEL), all the full-bridge FETs are turned off regardless of the PWM inputs. The IC remains in hiccup mode for a period equal to 10ms typically and then attempts to restart. Once the OCP condition removed, SC9608 exits hiccup mode and goes back to normal operation. The over current point is programmable by register (DTX_HSOC_SET).

9.14 Over-Voltage Protection (OVP)

Both the AVIN and PVIN pins implement the over-voltage protection function. When an OVP fault triggered, generate the interrupt signal to inform MCU the OVP condition for the further processing. The AVIN over-voltage protection is adjustable for 6V to 15V by register DAVOV_CFG [1:0]. The PVIN over voltage is about 15V with 1V hysteresis.

9.15 Over Temperature Protection (OTP)

The SC9608 over temperature protection includes OT warning and OT shutdown. When the die temperature rises over the thermal warning temperature, an alert signal will indicate the OT status. The OT warning point is programmable by register DTSW_CFG [2:0].

When the silicon die temperature exceeds 150℃, the SC9608 shuts down and it does not recover until the die temperature drop below 130℃.

10 Layout Guide

Here are the guidelines to follow:

- Make routing loop as small as possible, especially the power loop, to minimize EMI noises.
- Widen the copper between SW1, SW2 and LC tank, because high current in the LC tank can cause power losses on the traces and hence low efficiency. Moreover, the PVIN1/2 routing should be as wide as possible.
- Place BST1/2 bootstrap capacitors and series resistors close to the chip. Minimize the routing loop.
- Place small-size input capacitors as close as possible between the PVIN1/2 pins and PGND pin. These capacitors can effectively filter out high-frequency noises due to their low ESR and ESL.
- Separate the analog-ground plane from the power-ground plane, and use only one point to join them, best to connect the AGND pin to PGND pin at the bottom of IC as the black circle indicate in figure 6.
- Keep analog-ground plane and power-ground plane low impedance. Use as much copper as possible.

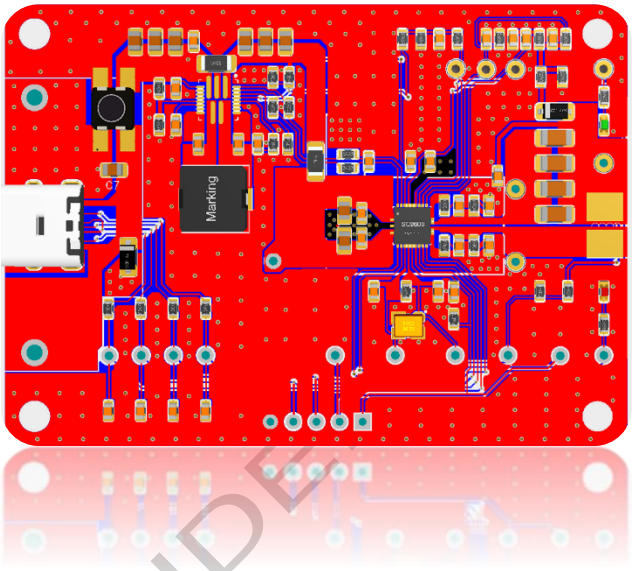


Fig6. Top Layer

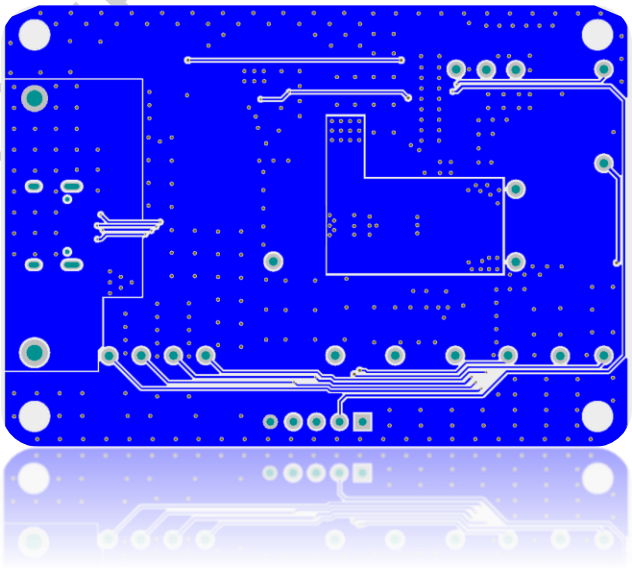


Fig7. Bottom Layer

11 Register Maps

MODULE	REGISTER NAME	ADDRESS	REGISTER DESCRIPTION
TIMER0	T0CTRL	0x4000_0000	Timer0 control register
	T0CNT	0x4000_0004	Timer0 count register
	T0CCR0	0x4000_0008	Timer0 compare register
TIMER1	T1CTRL	0x4000_1000	Timer1 control register
	T1CNT	0x4000_1004	Timer1 count register
	T1CCR0	0x4000_1008	Timer1 compare register 0
	T1CCR1	0x4000_100C	Timer1 compare register 1
TIMER2	T2CTRL	0x4000_2000	Timer2 control register
	T2CNT	0x4000_2004	Timer2 count register
	T2CCR0	0x4000_2008	Timer2 compare register 0
	T2CCR1	0x4000_200C	Timer2 compare register 1
PWMA	PWMA_CTRL	0x4000_3000	PWM control register
	PWMA_CNT	0x4000_3004	PWM count register
	PWMA_PERIOD	0x4000_3008	PWM period register
	PWMA_DUTY	0x4000_300C	PWM duty register
	PWMA_DEADTIME	0x4000_3010	PWM dead time register
	PWMA_PHASE	0x4000_3014	PWM phase register
GPIO	GPIOIN	0x4000_6000	GPIO input status register
	GPIOOUT	0x4000_6004	GPIO output status register
	GPIODIR	0x4000_6008	GPIO direction register
	GPIOAEN	0x4000_600C	GPIO analog function enable register
	GPIORPU	0x4000_6010	GPIO pull-up enable register
	GPIORPD	0x4000_6014	GPIO pull-down enable register
	GPIOIE	0x4000_6018	GPIO interrupt enable register
	GPIOIF	0x4000_601C	GPIO interrupt flag register
	GPIOM0	0x4000_6020	GPIO interrupt mode configure register
	GPIOM1	0x4000_6024	GPIO interrupt mode configure register
	IO_MUX	0x4000_6028	IO mux function configure register
WDT	WDT_CNT	0x4000_7000	Watch dog count register
	WDT_CTRL	0x4000_7004	Watch dog control register
	WDT_LOCK	0x4000_7008	Watch dog lock register
	WDT_INIT	0x4000_700C	Watch dog count value register
UART	UART_SBUF	0x4000_8000	UART buffer register
	UART_CTRL	0x4000_8004	UART control register
ADC	ADC_CTRL	0x4000_9000	ADC control register
	ADC_STATUS	0x4000_9004	ADC status register
	ADC_DATA	0x4000_9008	ADC result register
PMU	PMU_CTRL	0x4000_D000	PMU configuration register

	WAKEUP_EN	0x4000_D004	Sleep mode wakeup register
	CLK_CTRL	0x4000_D008	Block clock enable register
	DUMMY_REG	0x4000_D00C	Dummy register
	CHIP_ID	0x4000_D010	Chip ID register
	PMU_IE	0x4000_D014	PMU interrupt control register
	PMU_IF	0x4000_D018	PMU interrupt flag register
	XTAL_CTRL	0x4000_D01C	External crystal oscillator control register
	UIRC_CTRL	0x4000_D020	42M RC oscillator control register
ANALOG	ANA_IE	0x4001_A000	Analog interrupt enable register
	ANA_IF	0x4001_A004	Analog interrupt flag register
	ANA_STATUS	0x4001_A008	Analog status register
	ANA_CONF	0x4001_A00C	Analog configuration register
	ANA_CTRL	0x4001_A010	Analog control register
	ANA_QDET	0x4001_A014	Q_DET configuration register
	ANA_ISENSE	0x4001_A018	I sense configuration register
	ANA_PROTECT	0x4001_A01C	Protect configuration register
	ANA_BRIDGE	0x4001_A020	Full bridge configuration register
ASK_DEMOD	ASK_DM_DGL	0x4001_D000	DEMOD deglitch time register
	ASK_DM_CTRL	0x4001_D004	DEMOD control register
	ASK_DM_IE	0x4001_D008	DEMOD interrupt enable register
	ASK_DM_IF	0x4001_D00C	DEMOD interrupt flag register
	ASK_DM0_CNT	0x4001_D010	DEMOD channel0 count register
	ASK_DM0_CNT	0x4001_D014	DEMOD channel1 count register
	ASK_DM0_CAP	0x4001_D020	DEMOD channel0 capture register
	ASK_DM1_CAP	0x4001_D024	DEMOD channel1 capture register
	ASK_DM_CONF	0x4001_D030	DEMOD configuration register
SYS	SYS_INIT0	0x6000_0000	System initialization configuration register0
	SYS_INIT1	0x6000_0004	System initialization configuration register1
	BOOT_CTRL	0x6000_0008	Bootloader control register

Table 1.T0CTRL Register(Address=0x4000_0000h)

Bit	Name	Type	Reset	Notes
31	T0EN	R/W	0h	Timer0 enable 1：enable 0：disable
30:29	CLK_SRC[1:0]	R/W	0h	Select Timer0 clock source 00：LIRC_CLK（32KHz） 01：HIRC_CLK（24MHz） 10：UIRC_CLK（42MHz） 11：XTAL
28	T0_IO_EN	R/W	0h	Output timer0 overflow signal to GPIO enable 1: enable 0: disable
27	T0_IE	R/W	0h	Timer0 interrupt enable 1: enable 0: disable
26	T0_POLY	R/W	0h	Timer0 initial state
25	T0_IF	R/W	0h	Timer0 interrupt flag
24:7	RESERVED	N/A	N/A	
6:0	TM0_CLK_SCALE[6:0]	R/W	0h	Timer0 clock division T0_CLK=clock source / (tm0_clk_scale+1)

Table 2 T0CNT Register(Address=0x4000_0004h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	T0_COUNT[15:0]	R	FFFFh	Timer0 count register

Table 3.T0CCR0 Register(Address=0x4000_0008h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	AUTO_LOAD	R/W	FFFFh	Timer0 auto load register

Table 4.T1CTRL Register(Address=0x4000_1000h)

Bit	Name	Type	Reset	Notes
31	T1_EN	R/W	0h	1：Enable Timer1 0：Disable Timer1
30:29	CLK_SRC[1:0]	R/W	0h	Select Timer1 CLK source： 00：LIRC_CLK（32KHz） 01：HIRC_CLK（24MHz） 10：UIRC_CLK（42MHz） 11：XTAL
28	T1_IO_EN	R/W	0h	Output timer1 overflow signal to GPIO enable 1: enable 0: disable
27	T1_IE	R/W	0h	Timer1 interrupt enable
26	T1_POLY	R/W	0h	Timer1 initial state
25	T1_IF	R/W	0h	Timer1 interrupt flag
24	T1_IO_SEL	R/W	0h	Set PWM output IO 0: GPIO2 1: GPIO:3
23:7	RESERVED	N/A	N/A	
6:0	TM1_CLK_SCALE	R/W	0h	Timer1 clock division: t1_clk=clock source / (tm1_clk_scale+1)

Table 5.T1CNT Register(Address=0x4000_1004h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	COUNT	R	0h	Timer1 count register

Table 6.T1CCR0 Register(Address=0x4000_1008h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	CCR0[15:0]	R/W	0h	Timer1 capture/compare register 0

Table 7. T1CCR1 Register(Address=0x4000_100Ch)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	CCR1[15:0]	R/W	0h	Timer1 capture/compare register 1

Table 8. T2CTRL Register(Address=0x4000_2000h)

Bit	Name	Type	Reset	Notes
31	T2_EN	R/W	0h	1：Enable timer2 0：Disable timer2
30:29	CLK_SRC[1:0]	R/W	0h	Select Timer1 CLK source： 00：LIRC_CLK（32KHz） 01：HIRC_CLK（24MHz） 10：UIRC_CLK（42MHz） 11：XTAL
28	T2_IO_EN	R/W	0h	Send t2ov to GPIO
27	T2_IE	R/W	0h	Timer2 interrupt enable

26	T2_POLY	R/W	0h	Timer2 output polarity control
25	T2_IF	R/W	0h	Timer2 interrupt flag
24	T2_IO_SEL	R/W	0h	Set PWM output IO 0: GPIO2 1: GPIO3
23:7	RESERVED	N/A	N/A	
6:0	TM2_CLK_SCALE	R/W	0h	Timer2 clock division t2_clk=clock source / (tm2_clk_scale+1)

Table 9. T2CNT Register(Address=0x4000_2004h)

Bit	Name4	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	COUNT	R	0h	Timer2 count register

Table 10.T2CTRL Register(Address=0x4000_2008h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	CCR0[15:0]	R/W	0h	Timer2 capture/compare register 0

Table 11.T2CCR1 Register(Address=0x4000_200Ch)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	CCR1[15:0]	R/W	0h	Timer2 capture/compare register 1

Table 12.PWMA_CTRL Register(Address=0x4000_3000h)

Bit	Name	Type	Reset	Notes
31	PWMA_EN	R/W	0h	1：PWMA enable

				0：PWMA disable
30:29	PWMA_CLK_SRC[1:0]	R/W	0h	Select PWMA clock source 00：32K 01：24M 10：42M 11：XTAL
28:27	PWMA_RF_CFG[1:0]	R/W	0h	PWMA refresh cycle 00：256 01：128 10：64 11：32
26	PWMA_IF	R/W	0h	PWMA interrupt enable
25	PWMA_IE	R/W	0h	PWMA interrupt enable
24	PWMA_MODE	R/W	0h	Set PWMA mode 0：Duty mode 1：Phase mode
23	PWMA_REFRESH	W	N/A	Refresh PWMA
22:15	RESERVED	N/A	N/A	
14	PWM0_IO_EN	R/W	0h	1：PWMA0 GPIO3 output enable 0：disable
13	PWM0_EN	R/W	0h	1：PWMA0 enable 0：PWMA0 disable
12	PWM0_POLY	R/W	0h	1：PWMA0 default high 0：PWMA0 default low
11	RESERVED	N/A	N/A	

10	PWM1_IO_EN	R/W	0h	1：PWMA1 GPIO4 output enable 0：disable
9	PWM1_EN	R/W	0h	1：PWMA1 enable 0：PWMA1 disable
8	PWM1_POLY	R/W	0h	1：PWMA1 default high 0：PWMA1 default low
7	RESERVED	N/A	N/A	
6:0	PWM_CLK_SCALE[6:0]	R/W	0h	PWMA clock division PWMA_CLK = source clock / (tm2_clk_scale+1)

Table 13.PWMA_CNT Register(Address=0x4000_3004h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	PWM_COUNT	R	0h	PWMA count value

Table 14.PWMA_PERIOD Register(Address=0x4000_3008h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	PWM_PERIOD	R/W	0h	PWMA period value

Table 15.PWMA_DUTY Register(Address=0x4000_300Ch)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	PWM_DUTY	R/W	0h	PWMA duty value

Table 16.PWMA_DEADTIME Register(Address=0x4000_3010h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	PWM_DEADTIME	R/W	0h	PWM dead time value

Table 17.PWMA_PHASE Register(Address=0x4000_3014h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	PWM_PHASE[15:0]	R/W	0h	PWMA phase value

Table 18.GPIOIN Register(Address=0x4000_6000h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_IN[9:0]	R	0h	Input value of the corresponding GPIO[x] port

Table 19.GPIOOUT Register(Address=0x4000_6004h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_OUT[9:0]	R/W	0h	output value of the corresponding GPIO[x]

Table 20.GPIODIR Register(Address=0x4000_6008h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_DIR[9:0]	R/W	0h	Set GPIO[x] port direction 1：output 0：input

Table 21.GPIOAEN Register(Address=0x4000_600Ch)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_AEN[9:0]	R/W	0h	GPIO[x] analog input enable 1: analog input enable 0: analog input disable

Table 22.GPIORES Register(Address=0x4000_6010h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_RPU	R/W	0h	GPIO[x] pull up/down resistance enable 1: GPIO pull up/down enable 0: GPIO pull up/down disable

Table 23.GPIORUD Register(Address=0x4000_6014h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_RPD[9:0]	R/W	0h	Select GPIO[x] pull resistance direction 1：pull up 0：pull down

Table 24.GPIOIE Register(Address=0x4000_6018h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_IE[9:0]	R/W	0h	GPIO[x] interrupt configuration 1: GPIO input/wake-up interrupt enable 0: GPIO input/wake-up interrupt disable

Table 25.GPIOIF Register(Address=0x4000_601Ch)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_IF[9:0]	R/W	0h	GPIO[x] interrupt flag

Table 26.GPIOM0 Register(Address=0x4000_6020h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_M0[9:0]	R/W	0h	GPIO[x] input interrupt trigger mode 0: positive edge 1: negative edge

Table 27.GPIOM1 Register(Address=0x4000_6024h)

Bit	Name	Type	Reset	Notes
	RESERVED	N/A	N/A	
9:0	GPIO_M1[9:0]	R/W	0h	GPIO[x] input interrupt trigger mode 0: select by M0 1: all edge

Table 28 IO_MUX Register(Address=0x4000_6028h)

Bit	Name	Type	Reset	Notes
31	QDET_IO_EN	R/W	0x00	pin 5(GP5) enable QDET IO
30	NTC_IO_EN	R/W	0x00	pin 8(GP0) enable NTC current source output
29	XTAL_IO_EN	R/W	0x00	pin6&7 enable XTAL IO
28	ADC_IO6_EN	R/W	0x00	pin19(GP6) enable ADC IO
27	ADC_IO6_EN	R/W	0x00	pin18(GP8) enable ADC IO
26	DP_IO_EN	R/W	0x00	pin10(GP1) enable DP IO

25	DM_IO_EN	R/W	0x00	pin9(GP2) enable DM IO
24:4	Reserved	N/A	N/A	
3	IIC_IO_EN	R/W	0x01	enable IIC IO
2	JTAG_IO_EN	R/W	0x01	enable JTAG IO
1	TM_IO1	R/W	0x00	Reserved
0	TM_IO0	R/W	0x00	TEST_DATA mux out to GPIO9

Table 29.WDT_CNT Register(Address=0x4000_7000h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	COUNT	R	0h	WDT count value ,write 0x5F53435F to clear count

Table 30.WDT_CTRL Register(Address=0x4000_7004h)

Bit	Name	Type	Reset	Notes
31:9	RESERVED	N/A	N/A	
8	WDT_IF	R/W	0h	WDT interrupt flag
7:4	RESERVED	N/A	N/A	
3	WDT_IO_EN	R/W	0h	1: WDT output IO enable 0: WDT output IO disable
2	WDT_RSTB_EN	R/W	0h	1: WDT reset enable 0: WDT reset disable
1	WDT_EN	R/W	0h	1: WDT enable 0: WDT disable
0	WDT_IE	R/W	0h	1: WDT interrupt enable 0: WDT interrupt disable

Table 31.WDT_LOCK Register(Address=0x4000_7008h)

Bit	Name	Type	Reset	Notes
31:0	LOCK	W	0h	Write 0x5F4E585F to unlock WDT all registers write operation

Table 32.WDT_INIT Register(Address=0x4000_7010h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	N/A	
15:0	WDT_INIT	R/W	0h	Set WDT count value

Table 33.UART_SBUF Register(Address=0x4000_8000h)

Bit	Name	Type	Reset	Notes
31:8	RESERVED	N/A	N/A	
7:0	SBUF	W	0h	Serial buffer

Table 34.UART_CTRL Register(Address=0x4000_8004h)

Bit	Name	Type	Reset	Notes
31	UART_EN	R/W	0h	1: UART enable 0: UART disable
30	TX_IO_EN	R/W	0h	1: UART output IO enable 0: UART output IO disable
29	UART_IE	R/W	0h	1: UART interrupt enable 0: UART interrupt disable
28:24	RESERVED	N/A	N/A	
23	FIFO_FULL	R	0h	FIFO full flag
22	FIFO_EMPTY	R	0h	FIFO empty flag
21:17	RESERVED	N/A	N/A	

16	UART_IF	R/W	0h	UART interrupt flag
15	RESERVED	N/A	N/A	
14:0	BAUDRATE[14:0]	R/W	208	Set the baud rate Baud rate = 24M/ BAUDRATE [14:0]

Table 35.ADC_CTRL Register(Address=0x4000_9000h)

Bit	Name	Type	Reset	Notes
31	ADC_START	W	0h	Write 1 to start ADC conversion
30:17	RESERVED	N/A	N/A	Reserved
16	ADC_EN	R/W	0h	1: ADC enable 0: ADC disable
15:11	RESERVED	N/A	N/A	
10:8	ADC_CH_SEL[2:0]	R/W	0h	Set ADC conversion channel
7:6	RESERVED	N/A	N/A	
5:4	ADC_FREQ_SEL[1:0]	R/W	0x11	ADC conversion frequency 00：1KHz 01：5KHz 10：10KHz 11：20KHz
3	ADC_PWM_BLK_DIS	R/W	0h	ADC PWM Block algorithm disable 1：Disable 0：Enable
2:1	ADC_PWM_BLK_SEL[1:0]	R/W	0h	ADC PWM Block Delay Time Select 00：9 ADC clock cycles 01：8 ADC clock cycles 10：7 ADC clock cycles

				11：6 ADC clock cycles
0	ADC_SYN_RST	R/W	0h	ADC software reset Write 1 to reset ADC Write 0 to release reset

Table 36.ADC_STATUS Register(Address=0x4000_9004h)

Bit	Name	Type	Reset	Notes
31:2	RESERVED	N/A	N/A	Reserved
1	ADC_READY	R	0h	ADC ready flag
0	ADC_BUSY	R	0h	ADC busy flag

Table 37.ADC_CH_DATA Register(Address=0x4000_9008h)

Bit	Name	Type	Reset	Notes
31:10	RESERVED	N/A	N/A	Reserved
9:0	ADC_CH_DATA[9:0]	R	0h	ADC conversion result

Table 38.WAKEUP_EN Register(Address=0x4000_D004h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	R/W	0h	
15	GPIO7_WAKEUP_EN	R/W	0h	1: GPIO7/8/9 wakeup enable 0: GPIO7/8/9 wakeup disable
14	GPIO6_WAKUEP_EN	R/W	0h	1: GPIO6 wakeup enable 0: GPIO6 wakeup disable
13	GPIO5_WAKEUP_EN	R/W	0h	1: GPIO5 wakeup enable 0: GPIO5 wakeup disable
12	GPIO4_WAKEUP_EN	R/W	0h	1: GPIO4 wakeup enable 0: GPIO4 wakeup disable
11	GPIO3_WAKEUP_EN	R/W	0h	1: GPIO3 wakeup enable 0: GPIO3 wakeup disable
10	GPIO2_WAKEUP_EN	R/W	0h	1: GPIO2 wakeup enable 0: GPIO2 wakeup disable
9	GPIO1_WAKEUP_EN	R/W	0h	1: GPIO1 wakeup enable 0: GPIO1 wakeup disable

8	GPIO0_WAKEUP_EN	R/W	0h	1: GPIO0 wakeup enable 0: GPIO0 wakeup disable
7	ANA_WAKEUP_EN[1]	R/W	0h	1: Analog wakeup enable 0: Analog wakeup disable
6	ANA_WAKEUP_EN[0]	R/W	0h	1: Analog wakeup enable 0: Analog wakeup disable
5	CC_TMR_WAKEUP_EN	R/W	0h	1: CC timer wakeup enable 0: CC timer wakeup disable
4	PMU_WAKEUP_EN	R/W	0h	1: PMU wakeup enable 0: PMU wakeup disable
3	WDT_WAKEUP_EN	R/W	0h	1: WDT wakeup enable 0: WDT wakeup disable
2	TM2_WAKEUP_EN	R/W	0h	1: timer2 wakeup enable 0: timer2 wakeup disable
1	TM1_WAKEUP_EN	R/W	0h	1: timer1 wakeup enable 0: timer1 wakeup disable
0	TM0_WAKEUP_EN	R/W	0h	1: timer0 wakeup enable 0: timer0 wakeup disable

Table 39.CLK_CTRL Register(Address=0x4000_D008h)

Bit	Name	Type	Reset	Notes
31:18	RESERVED	R/W	0h	
17	AHB_MTP_CLK_EN	R/W	0h	1: MTP clock enable 2: MTP clock disable
16	TRIM_CLK_EN	R/W	1h	1: TRIM clock enable 2: TRIM clock disable
15	BIST_CLK_EN	R/W	1h	1: BIST clock enable 2: BIST clock disable
14	ASK_DM_CLK_EN	R/W	0h	1: ASK_DM clock enable 2: ASK_DM clock disable
13	ANA_CLK_EN	R/W	0h	1: Analog clock enable 2: Analog clock disable
12	AFCP0_CLK_EN	R/W	0h	1: AFCP clock enable 2: AFCP clock disable
11	DPDM0_CLK_EN	R/W	0h	1: DPDM clock enable 2: DPDM clock disable
10	PD_CLK_EN	R/W	0h	1: PD clock enable 2: PD clock disable
9	CC_CLK_EN	R/W	0h	1: CC clock enable 2: CC clock disable
8	PMU_CLK_EN	R/W	1h	1: PMU clock enable 2: PMU clock disable
7	M_IIC_CLK_EN	R/W	0h	1: IIC master clock enable 2: IIC master clock disable
6	ADC_CLK_EN	R/W	0h	1: ADC clock enable 2: ADC clock disable

5	UART0_CLK_EN	R/W	0h	1: UART clock enable 2: UART clock disable
4	WDT_CLK_EN	R/W	1h	1: WDT clock enable 2: WDT clock disable
3	PWMA_CLK_EN	R/W	0h	1: PWMA clock enable 2: PWMA clock disable
2	TM2_CLK_EN	R/W	0h	1: Timer2 clock enable 2: Timer2 clock disable
1	TM1_CLK_EN	R/W	0h	1: Timer1 clock enable 2: Timer1 clock disable
0	TM0_CLK_EN	R/W	0h	1: Timer0 clock enable 2: Timer0 clock disable

Table 40. DUMMY_REG Register(Address=0x4000_D00Ch)

Bit	Name	Type	Reset	Notes
31:16	DUMMY_IN[15:0]	R	0h	DUMMY IN
15:0	DUMMY_OUT[15:0]	R/W	0h	DUMMY OUT

Table 40. CHIP_ID Register(Address=0x4000_D010h)

Bit	Name	Type	Reset	Notes
31:4	RESERVED	N/A	N/A	Reserved
3:0	CHIP_ID[3:0]	R	0h	CHIP ID

Table 41. PMU_IE Register(Address=0x4000_D014h)

Bit	Name	Type	Reset	Notes
31:2	RESERVED	N/A	N/A	Reserved
1	DUMMY15_IE	R/W	0h	DUMMY15 interrupt enable 1: enable 0: disable
0	DUMMY14_IE	R/W	0h	DUMMY14 interrupt enable 1: enable 0: disable

Table 42. PMU_IF Register(Address=0x4000_D018h)

Bit	Name	Type	Reset	Notes

31:2	RESERVED	N/A	N/A	Reserved
1	DUMMY15_IF	R/W	0h	DUMMY15_IN interrupt flag
0	DUMMY14_IF	R/W	0h	DUMMY14_IN interrupt flag

Table 43. XTAL_CTRL Register(Address=0x4000_D01Ch)

Bit	Name	Type	Reset	Notes
31:9	RESERVED	N/A	N/A	Reserved
8	XTAL_OK	R	0h	XTAL stable flag
7:1	RESERVED	N/A	N/A	Reserved
0	XTAL_EN	R/W	0h	XTAL enable

Table 44.UIRC_TRL Register(Address=0x4000_D020h)

Bit	Name	Type	Reset	Notes
31:9	RESERVED	N/A	N/A	Reserved
8	UIRC_OK	R	0h	UIRC startup complete flag
7:1	RESERVED	N/A	N/A	Reserved
0	UIRC_EN	R/W	0h	UIRC enable

Table 45. ANA_IE Register(Address=0x4001_A000h)

Bit	Name	Type	Reset	Notes
31:12	RESERVED	N/A	0x0	reserved
11	BRG_TX_HSOC_IE	R/W	0h	Full bridge OCP interrupt enable 1: enable 0: disable
10	QDET_IN_IE	R/W	0h	QDET interrupt enable 1: enable 0: disable

9	TSW_IE	R/W	0h	Over temperature warning interrupt enable 1: enable 0: disable
8	TSD_IE	R/W	0h	Over temperature protect interrupt enable 1: enable 0: disable
7:5	RESERVED	N/A	0x0	reserved
4	AVDRP_IE	R/W	0h	AVIN low voltage interrupt enable 1: enable 0: disable
3	PVOV_IE	R/W	0h	PVIN over voltage interrupt enable 1: enable 0: disable
2	RESERVED			
1	AVOV_IE	R/W	0h	AVIN over voltage interrupt enable 1: enable 0: disable
0	AVDPM_IE	R/W	0h	AVIN Dynamic power management interrupt enable 1: enable 0: disable

Table 46. ANA_IF Register(Address=0x4001_A004h)

Bit	Name	Type	Reset	Notes
31:12	RESERVED	N/A	0x0	reserved
11	BRG_TX_HSOC_IF	R/W	0h	Full bridge OCP interrupt flag
10	QDET_IN_IF	R/W	0h	QDET output interrupt flag
9	TSW_IF	R/W	0h	TSW interrupt flag
8	TSD_IF	R/W	0h	TSD interrupt flag
7:5	RESERVED			

4	AVDRP_IF	R/W	0h	AVDRP interrupt flag
3	PVOV_IF	R/W	0h	PVOV interrupt flag
2	RESERVED			
1	AVOV_IF	R/W	0h	AVOV interrupt flag
0	AVDPM_IF	R/W	0h	AVDPM interrupt flag

Table 47. ANA_STATUS Register(Address=0x4001_A008h)

Bit	Name	Type	Reset	Notes
31:12	RESERVED	N/A	0h	reserved
11	HSOC_ST	R/W	0h	Full bridge OCP status
10	QDET_OUT_ST	R/W	0h	QDET output status
9	TSW_ST	R/W	0h	Over temperature warning status
8	TSD_ST	R/W	0h	Over temperature protect status
7:5	RESERVED	N/A	0h	reserved
4	AVDRP_ST	R/W	0h	AVIN low voltage status
3	PVOV_ST	R/W	0h	PCIN over voltage status
2	RESERVED	N/A	0h	reserved
1	AVOV_ST	R/W	0h	AVIN over voltage status
0	AVDPM_ST	R/W	0h	AVIN Dynamic power management status

Table 48. ANA_CONF Register(Address=0x4001_A00Ch)

Bit	Name	Type	Reset	Notes
31:12	RESERVED	N/A	0x0	reserved
11:10	QDET_IN_DGL_SEL	R/W	0x01	QDET input deglitch time 00：5uS

				01：10uS 10：20uS 11：40uS
9:8	P_AVDRP_DGL_SEL	R/W	0x03	AVIN low voltage deglitch time 00：20uS 01：40uS 10：80uS 11：160uS
7:6	P_PVOV_DGL_SEL	R/W	0x03	PVIN over voltage deglitch time 00：20uS 01：40uS 10：80uS 11：160uS
4:3	RESERVED			
2	P_AVOV_DGL_SEL	R/W	0x03	AVIN over voltage deglitch time 0：32us 1：64us
1	RESERVED			
0	P_AVDPM_DGL_SEL	R/W	0x03	AVIN dynamic power management deglitch time 0：32us 1：64us

Table 49. ANA_CTRL Register(Address=0x4001_A010h)

Bit	Name	Type	Reset	Notes
31:3	RESERVED	N/A	0x0	reserved
2:1	NTC_ISEL	R/W	0h	NTC configuration

				00：INTC=100uA 01：INTC=20uA 10：INTC=4uA 11：INTC disable
0	EN_BG_2NDTC	R/W	0h	Second-order temperature compensation enable 0：disable 1：enable

Table 50. ANA_QDET Register(Address=0x4001_A014h)

Bit	Name	Type	Reset	Notes
31:2	RESERVED	N/A	0x0	reserved
1	QDET_BIASEN	R/W	0h	QDET bias enable 1: enable 0: disable
0	QDET_EN	R/W	0h	QDET function enable 1: enable 2: disable

Table 51. ANA_ISENSE Register(Address=0x4001_A018h)

Bit	Name	Type	Reset	Notes
31:2	RESERVED	N/A	0x0	reserved
1	CSNS_SEL20X	R/W	0x01	1: current sense use 20m ohms resistor 0: current sense use 10m ohms resistor
0	CSNS_EN	R/W	0h	Current sense enable

Table 52. ANA_PROTECT Register(Address=0x4001_A01Ch)

Bit	Name	Type	Reset	Notes

31:20	RESERVED	N/A	0x0	reserved
19	P_TSD_EN	R/W	0x01	Over temperature protection enable 1: enable 0: disable
18:16	P_TSW_CFG	R/W	0x07	High temperature configuration 000: 65C ~111: 125C
15:13	RESERVED	N/A	0x0	reserved
12	P_AVDRP_CFG	R/W	0h	AVIN drop voltage protect configuration 1: 11.5V 0: 8.5V
11:10	P_AVOV_CFG	R/W	0h	AVIN over voltage protect configuration 00: 6V 01: 10V 10: 13V 11: 15V
9:8	P_AVDPM_CFG	R/W	0h	Dynamic power management configuration 00: 4.2V 01: 4.4V 10: 4.6V 11: 4.8V
7:5	RESERVED	N/A	0x0	reserved
4	P_AVDPM_HYS	R/W	0h	Dynamic power management voltage hysteresis configuration 1: 400mV Hysteresis 0: 200mV Hysteresis
3	P_EN_AVDRP	R/W	0h	AVIN drop voltage protect enable 1: enable 0: disable
2	P_EN_PVOV	R/W	0h	PVIN over voltage protect enable 1: enable 0: disable

1	P_EN_AVOV	R/W	0x01	AVIN over voltage protect enable 1: enable 0: disable
0	P_EN_AVDPM	R/W	0h	Dynamic power management enable 1: enable 0: disable

Table 53. ANA_BRIDGE Register(Address=0x4001_A020h)

Bit	Name	Type	Reset	Notes
31:22	RESERVED	N/A	0h	reserved
21	TSD_EN	R/W	0x01	TSD control PWM full bridge enable 1: enable TSD control PWM 0: disable TSD control pwm
20:19	RESERVED	N/A	0h	reserved
18:16	DEAD_TIME	R/W	0x07	Full bridge driver dead timer configuration 000: 15nS 001: 25nS 010: 35nS 011: 45nS 100: 55nS 101: 65nS 110: 75nS 111: 85nS
15	HSOC_CLR	R/W	0h	Software clear OCP 1: clear OCP state 0: keep current state
14:12	HSOC_SET	R/W	0h	Full bridge OCP threshold configuration 000: 6A 001: 7A 010: 8A 011: 9A

				100: 10A 101: 11A 110: 12A 111: 13A
11	HSOC_CNT_SEL	R/W	0x01	Set the number of OCP cycles 1: 4 PWM cycles 0: 8 PWM cycles
10	HSOC_INTHICUP_EN	R/W	0x01	Hiccup enable control 1: hiccup after trigger OCP 0: disable
9	LOGIC_EN	R/W	0h	Full bridge logic enable 1: enable logic 0: disable logic
8	HSOC_EN	R/W	0h	Full bridge OCP enable 1: enable 0: disable
7:6	CFGSR_DRV2	R/W	0x02	SW2 low side FET slew rate configuration 00: slowest 01: slow 10: fast 11: faster
5:4	CFGSR_DRV1	R/W	0x02	SW1 low side FET slew rate configuration 00: slowest 01: slow 10: fast 11: faster
3	DIS_BTOK	R/W	0h	PWMA driver boot ok disable 1: disable boot ok 0: enable boot ok
2	BRG_EN_RVD2	R/W	0h	PWMA1 driver enable 0: disable

				1: enable
1	BRG_EN_RVD1	R/W	0h	PWMA0 driver enable 0: disable 1: enable
0	PWM_EN_HIZ	R/W	0h	PWM driver HIZ enable 1: enable HIZ 0: disable HIZ

Table 54. ASK_DM_DGL Register(Address=0x4001D000h)

Bit	Name	Type	Reset	Notes
31:14	RESERVED	N/A	0h	reserved
13:8	DM1_DGL[6:0]	R/W	0h	Current demod deglitch time 1~64us
7:6	RESERVED	N/A	0h	reserved
5:0	DM0_DGL[6:0]	R/W	0h	Voltage demod deglitch time 1~64us

Table 55. ASK_DM_CTRL Register(Address=0x4001D004h)

Bit	Name	Type	Reset	Notes
31:11	RESERVED	N/A	0h	reserved
10:9	DM1_MODE	R/W	0h	00: count++ at booth positive & negative edge save count in cap register 01: count++ at high level & clear in low level, negative edge save count in cap register 10: count++ at low level & clear in high level, positive edge save count in cap register 11: count++ at both positive & clear, negative edge save count in cap register
8	DM1_EN	R/W	0h	1: enable current de-modulation function
7:3	RESERVED	N/A	0h	reserved
2:1	DM0_MODE	R/W	0h	00: count++ at booth positive & negative edge save count in cap register

				01: count++ at high level & clear in low level, negative edge save count in cap register 10: count++ at low level & clear in high level, positive edge save count in cap register 11: count++ at both positive & clear, negative edge save count in cap register
0	DM0_EN	R/W	0h	1: enable voltage de-modulation function

Table 56. ASK_DM_IE Register(Address=0x4001D008h)

Bit	Name	Type	Reset	Notes
31:9	RESERVED	N/A	0h	reserved
8	DM1_IE	R/W	0h	1: enable current de-modulation interrupt 0: disable
7:1	RESERVED	N/A	0h	reserved
0	DM0_IE	R/W	0h	1: enable voltage de-modulation interrupt 0: disable

Table 57. ASK_DM_IF Register(Address=0x4001D00Ch)

Bit	Name	Type	Reset	Notes
31:10	RESERVED	N/A	0h	reserved
9	DM1_OV_IF	R	0h	current de-modulation overflow flag
8	DM1_CAP_IF	R	0h	current de-modulation capture flag
7:2	RESERVED	N/A	0h	reserved
1	DM0_OV_IF	R	0h	voltage de-modulation overflow flag
0	DM0_CAP_IF	R	0h	voltage de-modulation capture flag

Table 58. ASK_DM0_CNT Register(Address=0x4001D010h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	0h	reserved

15:0	DM0_CNT	R	0h	DM0 counter

Table 59. ASK_DM1_CNT Register(Address=0x4001D014h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	0h	reserved
15:0	DM1_CNT	R	0h	DM1 counter

Table 60. ASK_DM0_CAP Register(Address=0x4001D020h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	0h	reserved
15:0	DM0_CAP	R	0h	DM0 capture

Table 61. ASK_DM1_CAP Register(Address=0x4001D024h)

Bit	Name	Type	Reset	Notes
31:16	RESERVED	N/A	0h	reserved
15:0	DM1_CAP	R	0h	DM1 capture

Table 62. ASK_DM_CONF Register(Address=0x4001D030h)

Bit	Name	Type	Reset	Notes
31:15	RESERVED	N/A	0h	reserved
14:12	DM0_HYS	R/W	0h	voltage de-modulation comparator hysteresis 000: 5mV 001: 10mV 010: 20mV 011: 30mV 100: 40mV 101: 60mV 110: 80mV

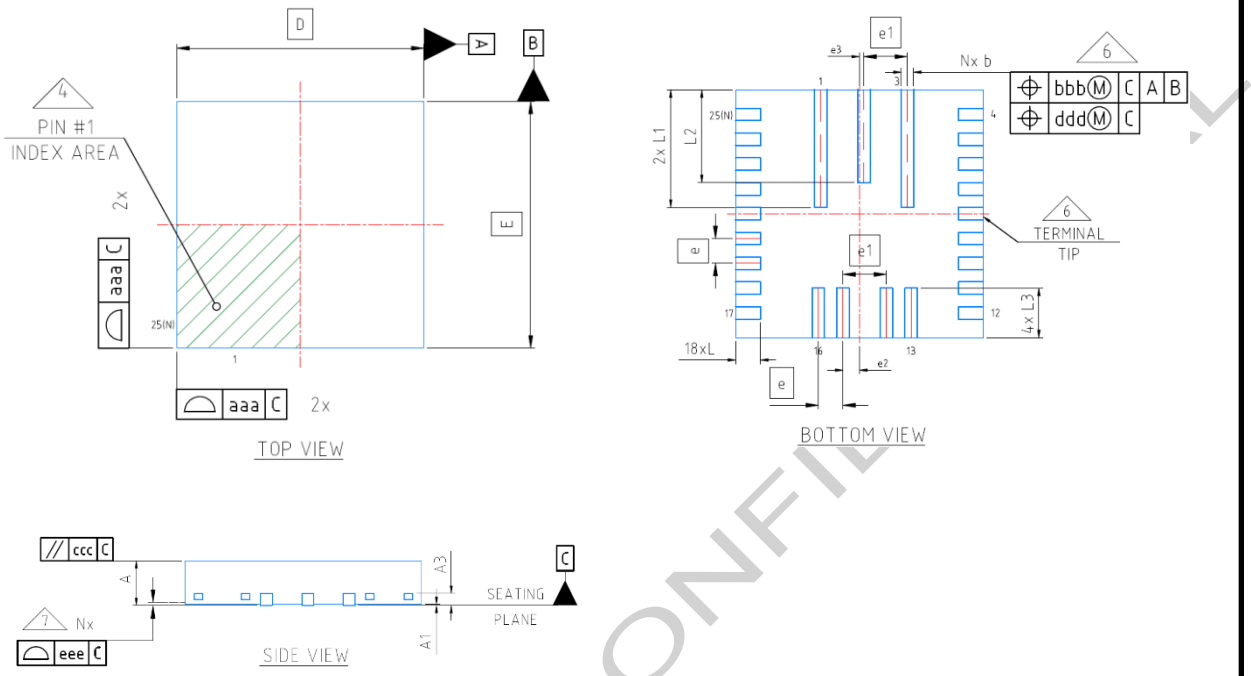
				111: 100mV
11:4	RESERVED	N/A	0h	reserved
3	DM_IDM_AZCVER	R/W	0h	current de-modulation auto-zero function enable
2:0	DM1_HYS	R/W	0h	current de-modulation comparator hysteresis 000: 5mV 001: 10mV 010: 20mV 011: 30mV 100: 40mV 101: 60mV 110: 80mV 111: 100mV

Table 63. SYS_INIT0 Register(Address=0x6000000h)

Bit	Name	Type	Reset	Notes
31:18	RESERVED	N/A	0h	reserved
17	cpu_clk_sel	R/W	0h	CPU clock select 0: 8M 1: 6M
16	jtag_dis	R/W	0h	jtag disable
15:0	RESERVED	N/A	0h	reserved

12 MECHANICAL DATA

FCQFN25L (4x4x0.75)



Dimension Table							
Thickness / Symbol	W			V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM	
A	0.70	0.75	0.80	0.80	0.90	1.00	
A1	0.00	0.02	0.05	0.00	0.02	0.05	
A3	---	0.203 Ref.	---	---	0.203 Ref.	---	
b	0.15	0.20	0.25	0.15	0.20	0.25	6
D	4.00 BSC			4.00 BSC			
E	4.00 BSC			4.00 BSC			
e	0.40 BSC			0.40 BSC			
e1	0.70 BSC			0.70 BSC			
e2	0.27 BSC			0.27 BSC			
e3	0.07 BSC			0.07 BSC			
L	0.30	0.40	0.50	0.30	0.40	0.50	
L1	1.80	1.90	2.00	1.80	1.90	2.00	
L2	1.40	1.50	1.60	1.40	1.50	1.60	
L3	0.70	0.80	0.90	0.70	0.80	0.90	
aaa	0.05			0.05			
bbb	0.10			0.10			
ccc	0.10			0.10			
ddd	0.05			0.05			
eee	0.08			0.08			
N	25						3
ND	3/4						5
NE	9						5
NOTES	1, 2						
LF PART NO.	446251						