SLM7888

160V 3-Phase Bridge Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 160 V max.
- **I_O+/-** 350 mA / 650 mA
- **V_{OUT}** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 130 ns / 150 ns
- **Deadtime (typ.)** 270 ns

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +160 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- 3.3 V, 5 V, and 15 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Cross-conduction prevention logic with Typ. 270ns dead time
- Available in SOIC-20L (WB) and TSSOP-20L (NB) packages

GENERAL DESCRIPTION

The SLM7888 is a high voltage, high speed power MOSFET and IGBT drivers with three independent high- and low-side referenced output channels for 3-phase applications.

Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

The logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic.

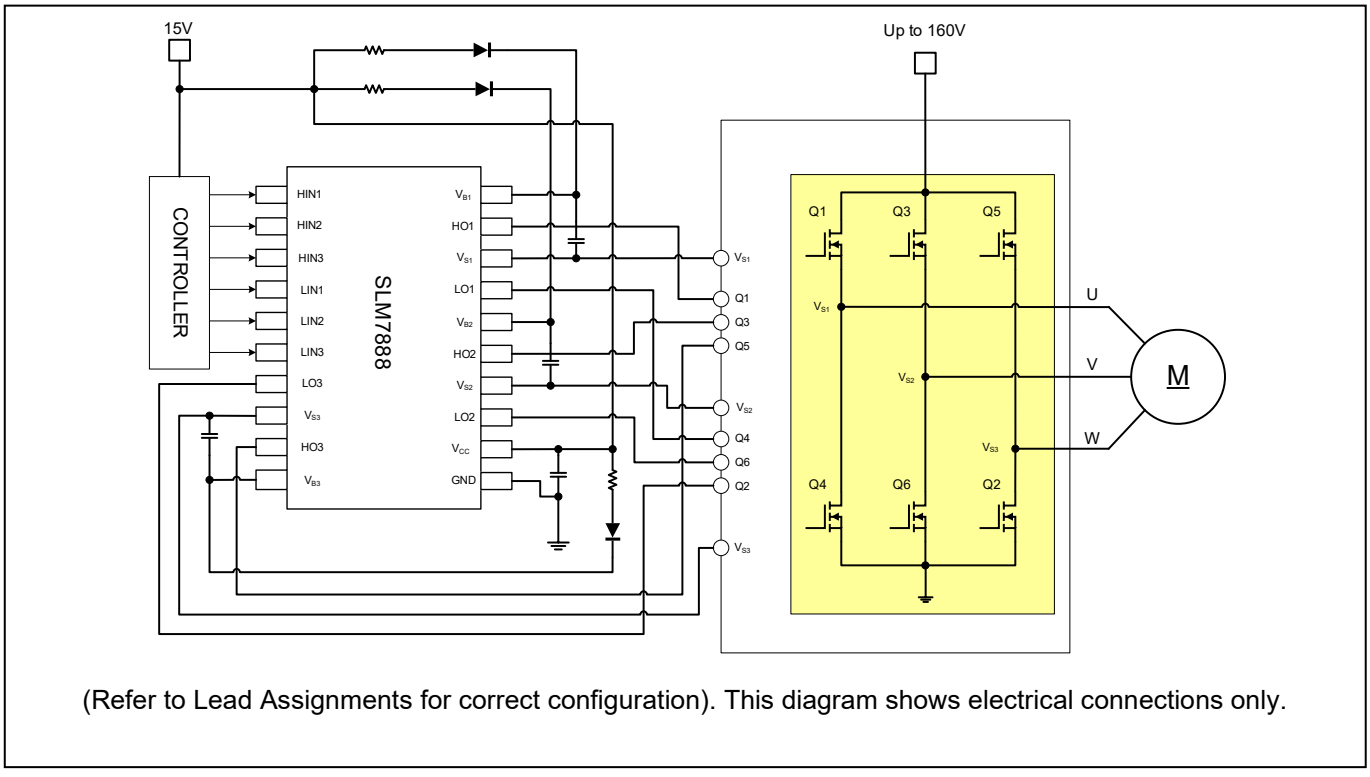
An advanced level-shift circuit allows high-side gate driver operation up to V_S = -9.8V for V_{BS} = 15V.

The UVLO circuits prevent malfunction when VDD and VBS are lower than the specified threshold voltage.

Propagation delays are matched to simplify use in high frequency applications.

The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 160 V.

TYPICAL APPLICATION CIRCUIT



(Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only.

Figure 1 Typical Application Circuit

PIN CONFIGURATION

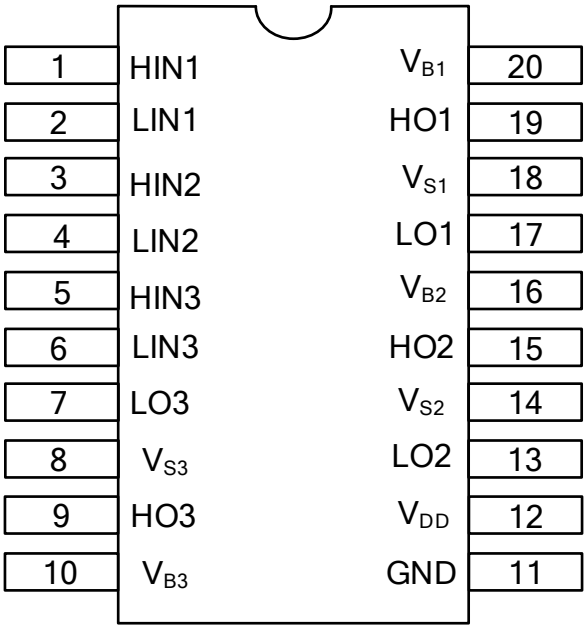
Package	Pin Configuration (Top View)
SOIC-20L (WB) TSSOP-20L (NB)	

Figure 2 Pin Configuration

PIN DESCRIPTION

No.	Pin	Description
1, 3, 5	HIN1, 2, 3	Logic input for high-side gate driver output (HO).
2, 4, 6	LIN1, 2, 3	Logic input for low-side gate driver output (LO).
19, 15, 9	HO1, 2, 3	High-side gate driver outputs.
17, 13, 7	LO1, 2, 3	Low-side gate driver outputs.
18, 14, 8	$V_{S1, 2, 3}$	High-side drivers floating supply offset.
20, 16, 10	$V_{B1, 2, 3}$	High-side drivers floating supply.
11	GND	Ground.
12	V_{DD}	Logic and all low-side gate drivers power supply.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM7888CH	SOIC-20L (WB), Pb-Free	1000/Reel
SLM7888MD	TSSOP-20I (NB), Pb-Free	4000/Reel

FUNCTIONAL BLOCK DIAGRAM

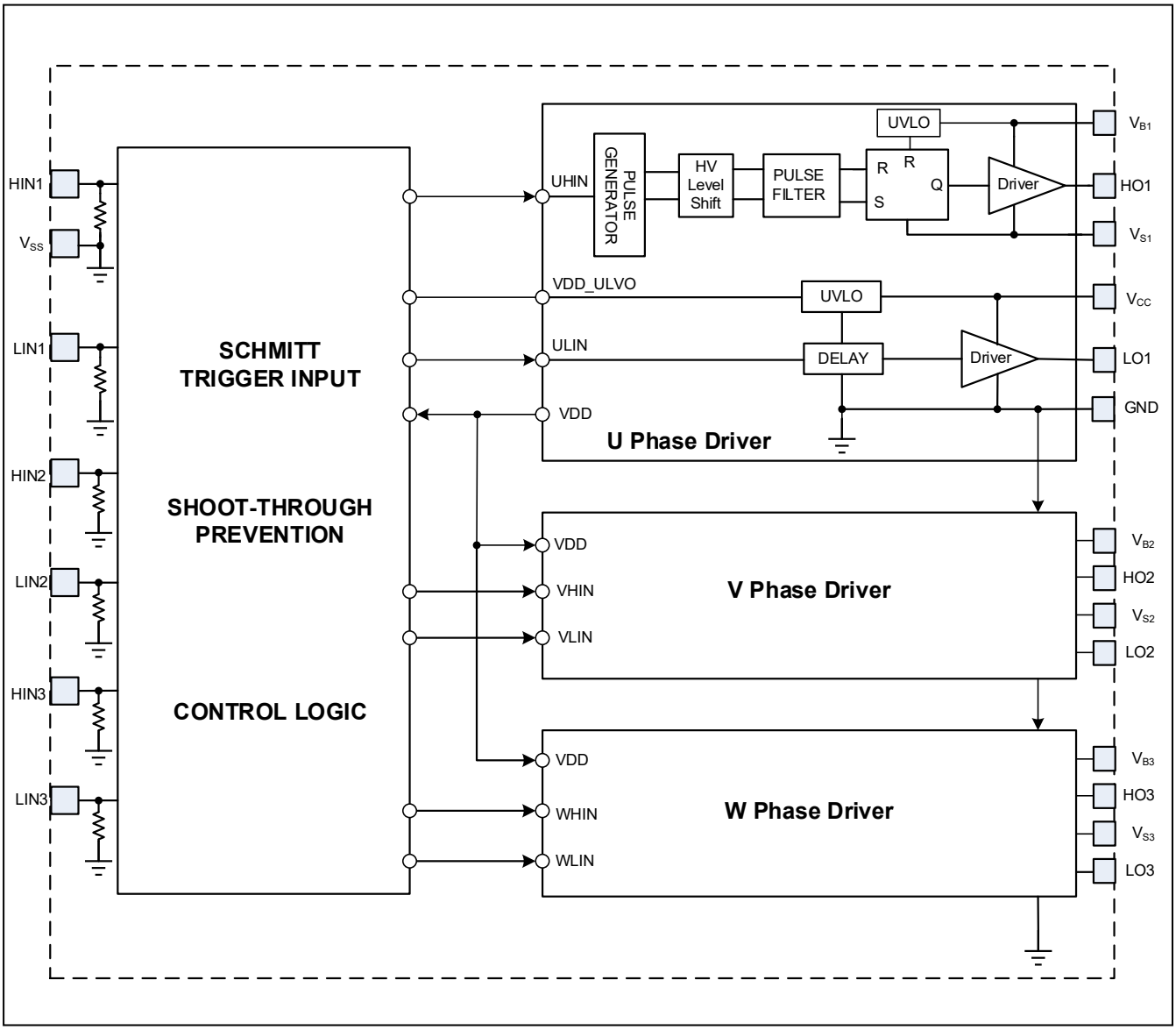


Figure 3 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	185	V
V_S	High-side floating supply offset voltage		$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
V_{HO}	High-side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{IN}	Logic input voltage (LIN, HIN)		- 0.3	V_{DD} + 0.3	
$V_{LO1,2,3}$	Low-side output voltage		-0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant +25°C$	SOIC-20L (WB)	---	1.5	W
		TSSOP-20L (NB)	---	1.2	
Rth_{JA}	Thermal resistance, junction to ambient	SOIC-20L (WB)	---	60	°C/W
		TSSOP-20L (NB)	---	75	
T_J	Junction temperature		-40	125	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

Note:
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATIONG CONDITIONS

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High-side floating supply voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High-side floating supply offset voltage	- 0.3	160	
$V_{HO1,2,3}$	High-side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low-side output voltage	GND	V_{DD}	
V_{DD}	Low-side and logic fixed supply voltage	10	20	
V_{IN}	Logic input voltage (LIN, HIN)	GND	V_{DD}	
T_A	Ambient temperature	- 40	125	°C

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, $V_{S1,2,3}$ = GND, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	130	220	ns
t_{off}	Turn-off propagation delay	V_S = 160 V	---	150	240	
t_r	Turn-on rise time		---	50	120	
t_f	Turn-off fall time		---	30	80	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	V_{IN} = 0 V & 5 V	100	270	440	
MT	Matching delay, HS & LS turn-on/off	External dead time > 400 ns	---	40	60	
MDT	Matching delay, max (t_{on}, t_{off}) – min (t_{on}, t_{off}), (t_{on}, t_{off} are applicable to all 3 channels)		---	25	50	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, $V_{BS1,2,3}$) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to GND and are applicable to all 6 channels (LIN, HIN). The V_O and I_O parameters are referenced to GND and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “0” input voltage (LIN, HIN)	V_{CC} = 10 V to 20V	2.5	---	---	V
V_{IL}	Logic “1” input voltage (LIN, HIN)		---	---	1.0	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	---	0.5	1.0	
V_{OL}	Low level output voltage, V_O		---	0.3	0.6	
V_S	Available negative V_S pin voltage for input signal propagation to H_O		---	- 9.8	- 7.0	
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} supply undervoltage positive going threshold		6.0	6.7	7.8	
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} supply undervoltage negative going threshold		5.4	6.2	7.0	
V_{DDUVH} V_{BSUVH}	V_{DD} and V_{BS} supply undervoltage lockout hysteresis		0.3	0.5	---	
I_{LK}	Offset supply leakage current	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 160 V	---	---	10	μA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	---	65	120	
I_{QDD}	Quiescent V_{DD} supply current		---	300	500	
I_{OPDD}	Operating V_{DD} supply current for each channel	$f_{LIN1,2,3}$ = 20 kHz, rms Value	---	500	900	
I_{OPBS}	Operating V_{BS} supply current for each channel	$f_{LIN1,2,3}$ = 20 kHz, rms Value	---	400	800	
I_{IN+}	Logic “1” input bias current	HIN1, 2, 3 = 5 V, LIN1, 2, 3 = 5 V	---	25	50	μA
I_{IN-}	Logic “0” input bias current	HIN1, 2, 3 = 0 V, LIN1, 2, 3 = 0 V	---	---	2	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, V_{IN} = V_{IH} PW ⩽ 10 μs	---	350	---	mA
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, V_{IN} = V_{IL} PW ⩽ 10 μs	---	650	---	
R_{IN}	Input pull-down resistance		150	200	20	kΩ

TYPICAL CHARACTERISTICS

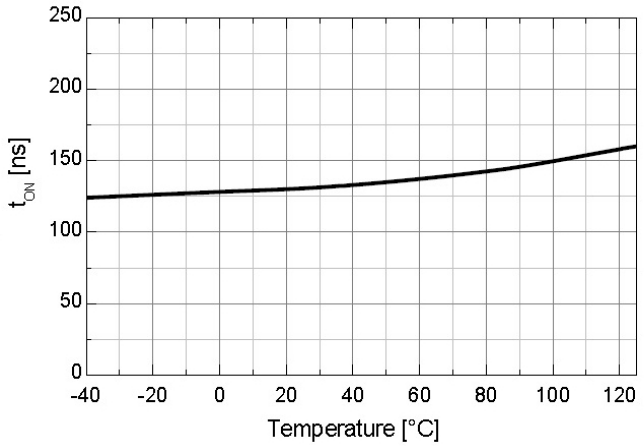


Figure 4 Turn-on Propagation Delay vs. Temp.

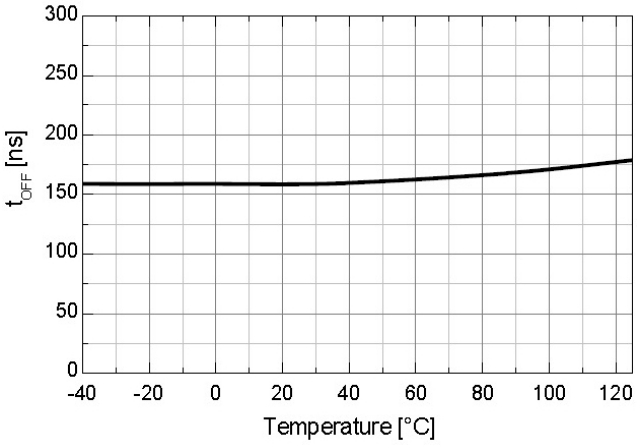


Figure 5 Trun-off Propagation Delay vs. Temp.

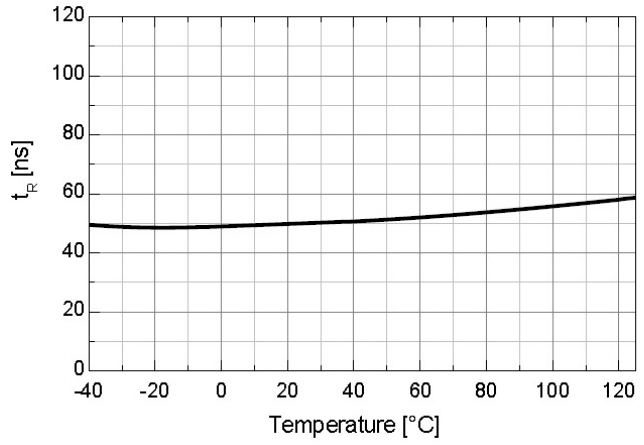


Figure 6 Turn-on Rise Time vs. Temp.

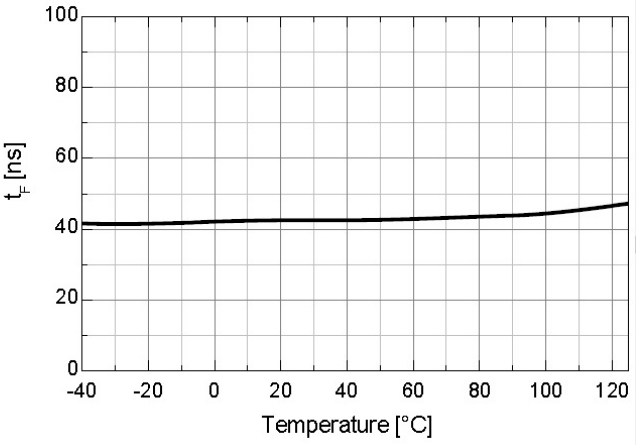


Figure 7 Trun-off Fall Time vs. Temp.

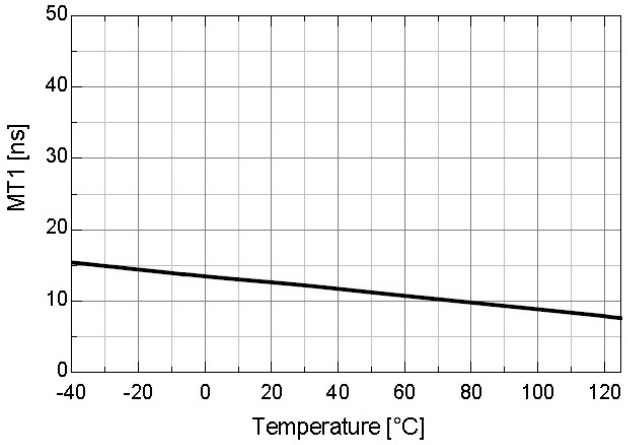


Figure 8 Turn-on Delay Matching vs. Temp.

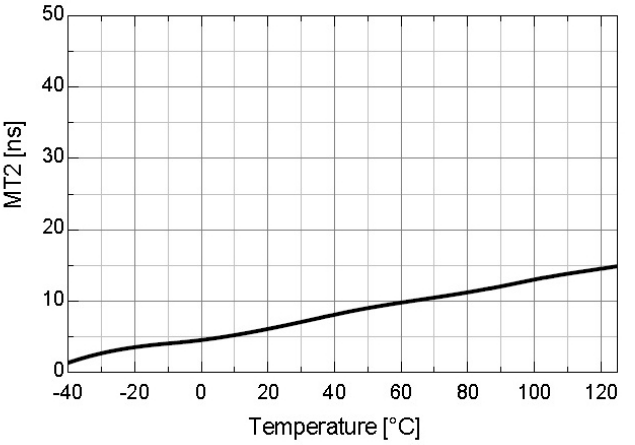


Figure 9 Trun-off Delay Matching vs. Temp.

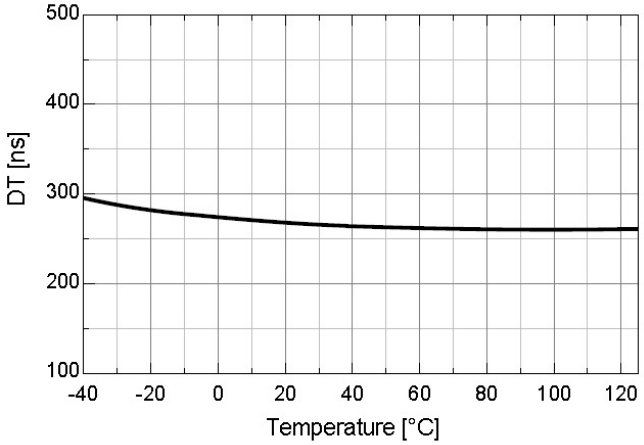


Figure 10 Dead Time vs. Temp.

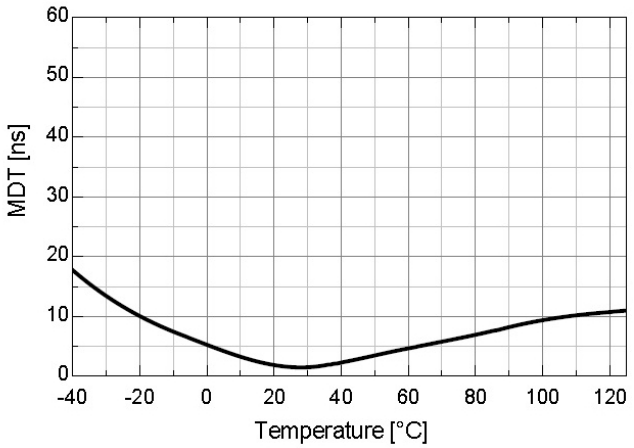


Figure 11 Dead Time Matching vs. Temp.

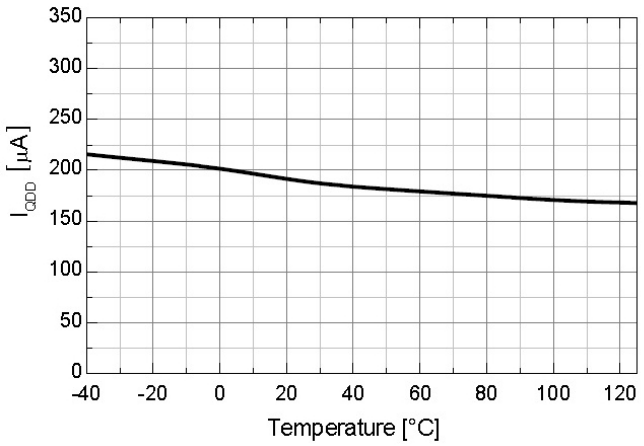


Figure 12 Quiescent V_{DD} Supply Current vs. Temp.

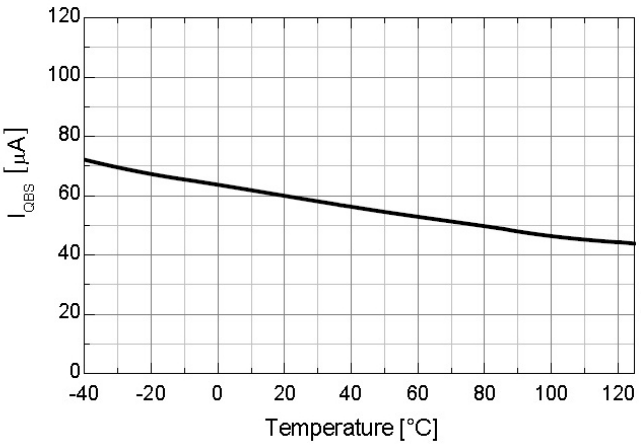


Figure 13 Quiescent V_{BS} Supply Current vs. Temp.

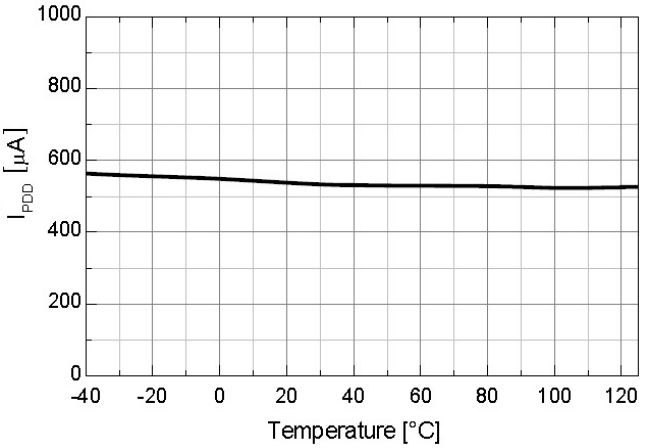


Figure 14 Operating V_{DD} Supply Current vs. Temp.

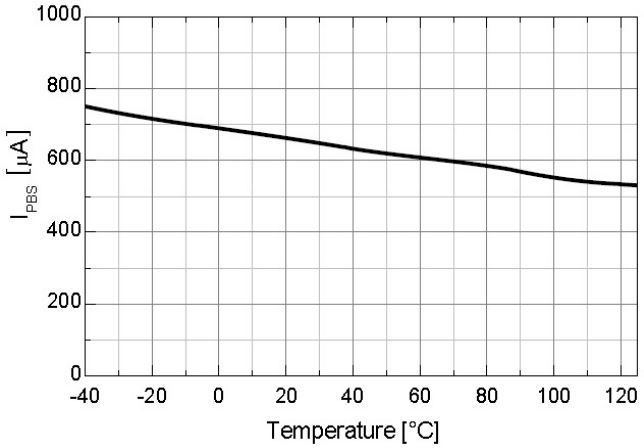


Figure 15 Operating V_{BS} Supply Current vs. Temp.

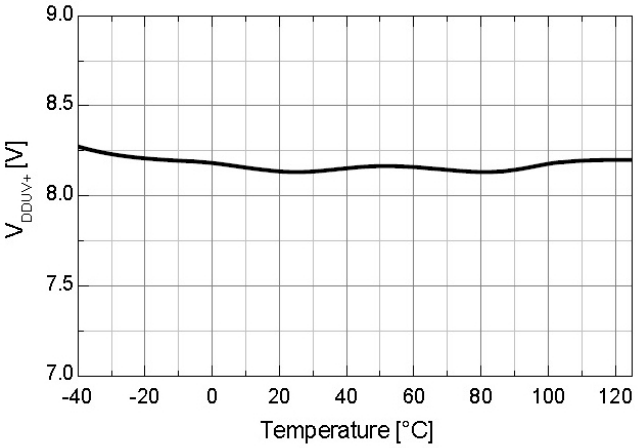


Figure 16 V_{DD} UVLO+ vs. Temp.

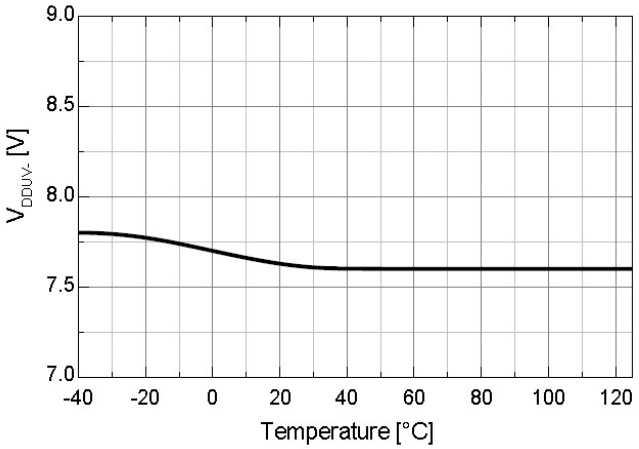


Figure 17 V_{DD} UVLO- vs. Temp.

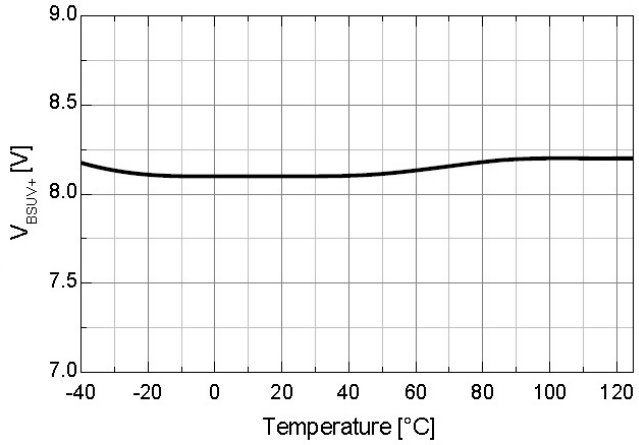


Figure 18 V_{BS} UVLO+ vs. Temp.

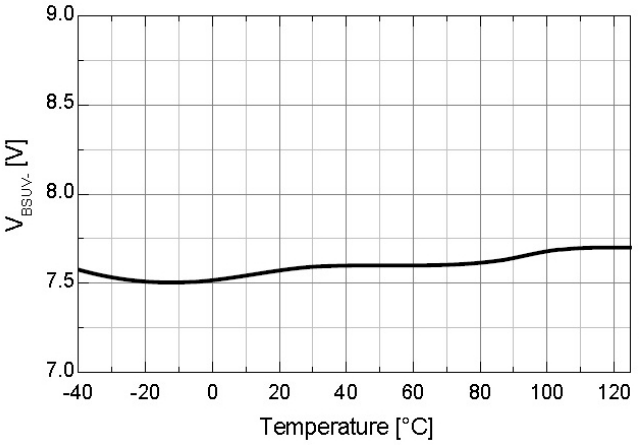


Figure 19 V_{BS} UVLO- vs. Temp.

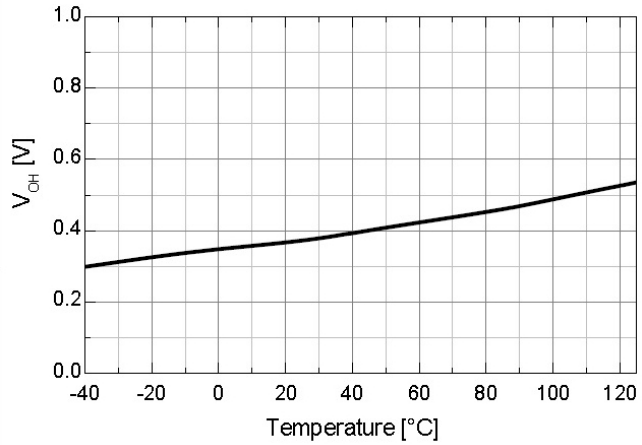


Figure 20 High-level Output Voltage vs. Temp.

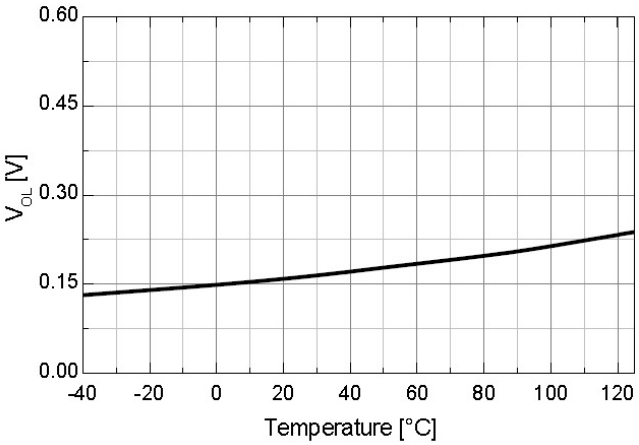


Figure 21 Low-level Output Voltage vs. Temp.

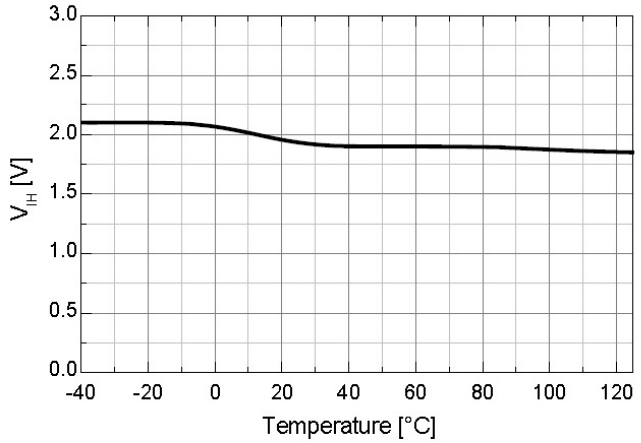


Figure 22 Logic High Input Voltage vs. Temp.

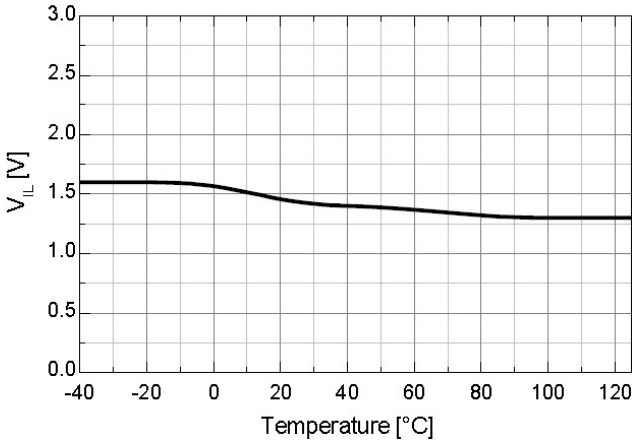


Figure 23 Logic High Input Voltage vs. Temp.

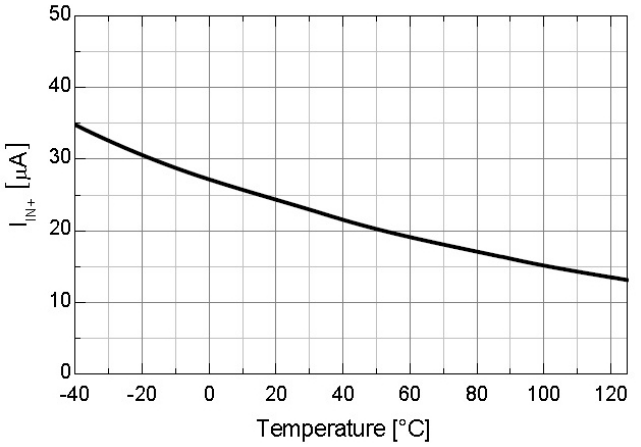


Figure 24 Logic High Input Bias Current vs. Temp

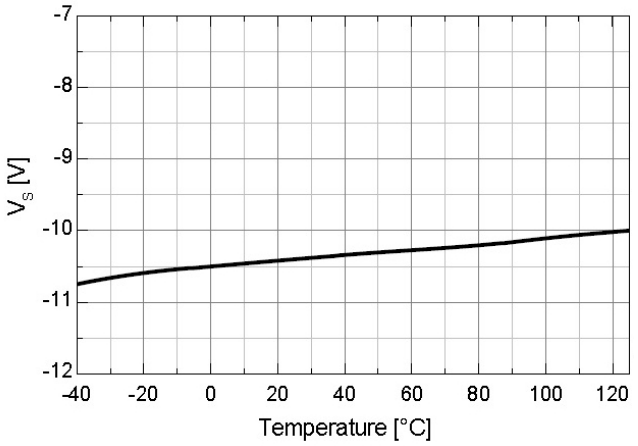


Figure 25 Allowable Negative V_S Voltage vs. Temp.

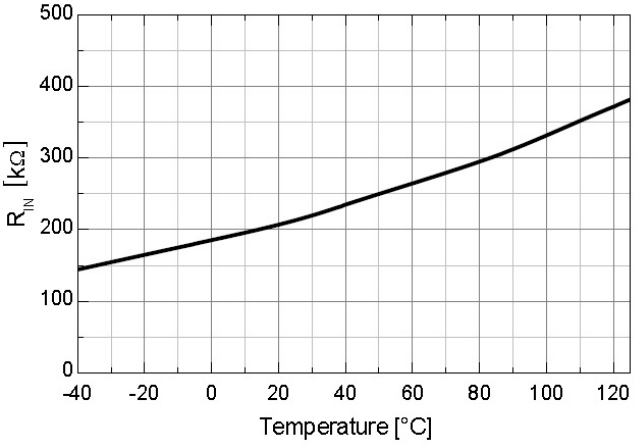


Figure 26 Input Pull-down Resistance vs. Temp.

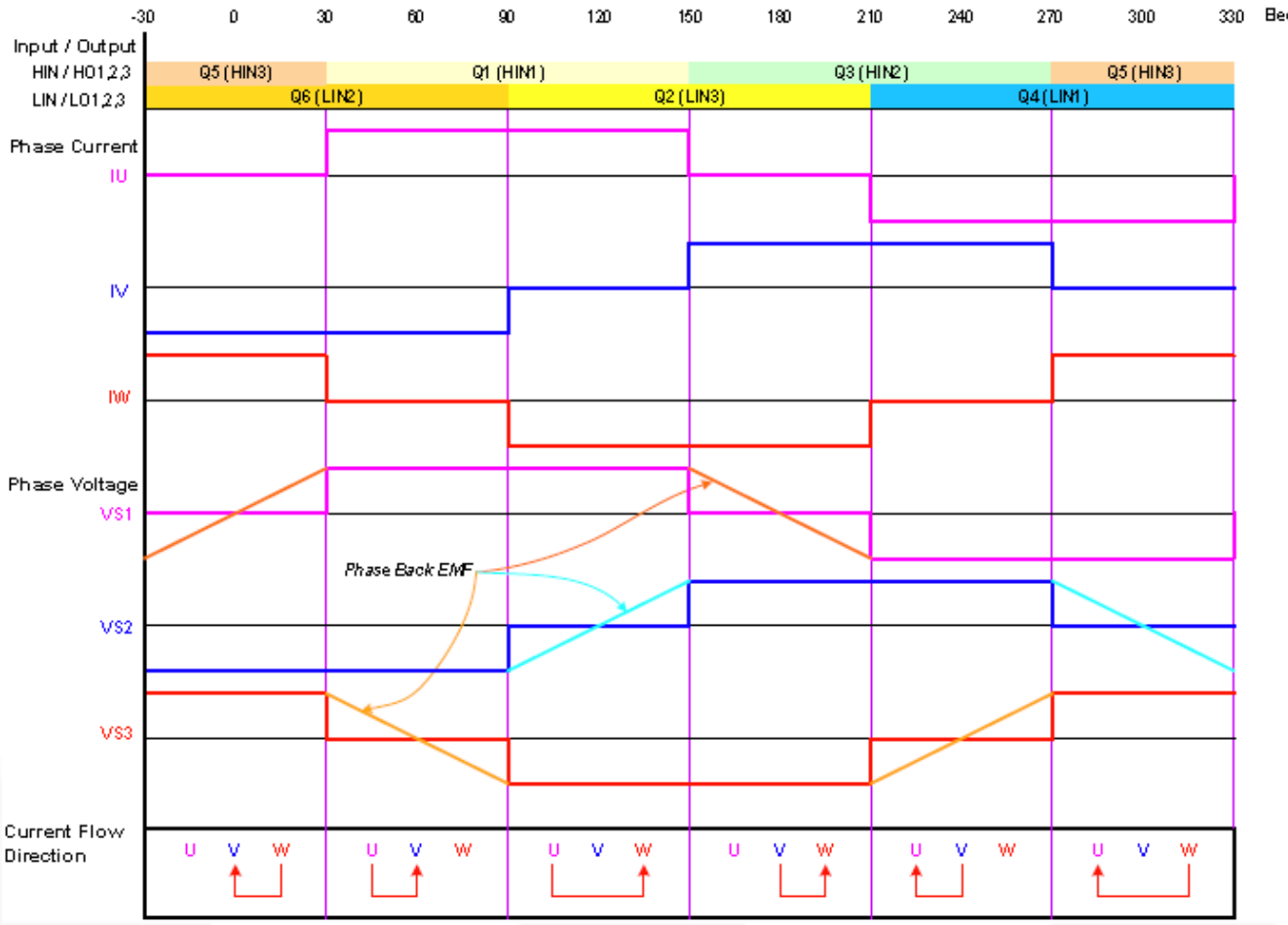


Figure 27 120° Communication Operation Waveforms for 3-Phase BLDC Motor Application

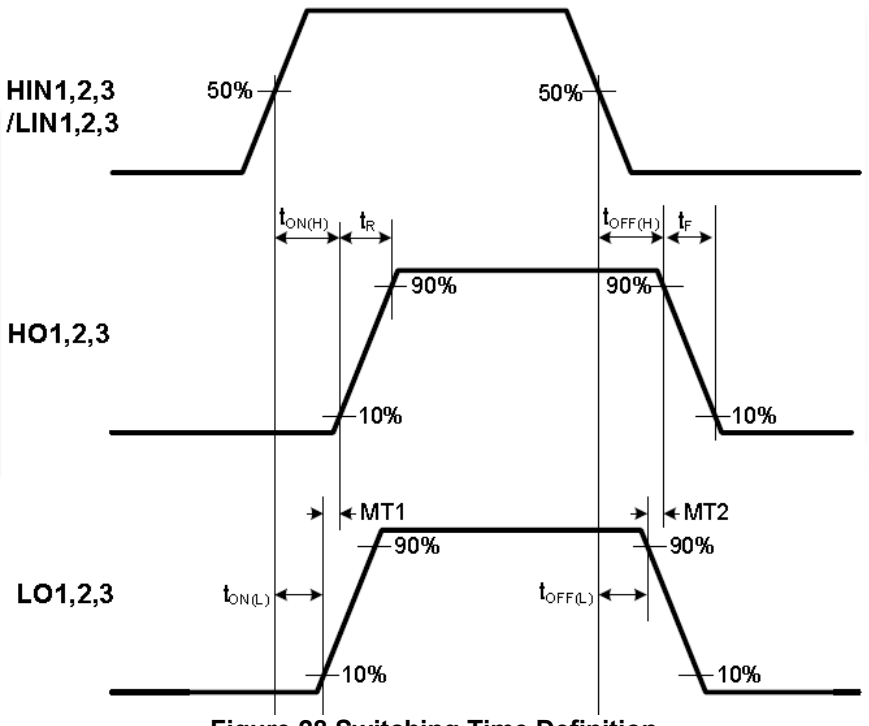
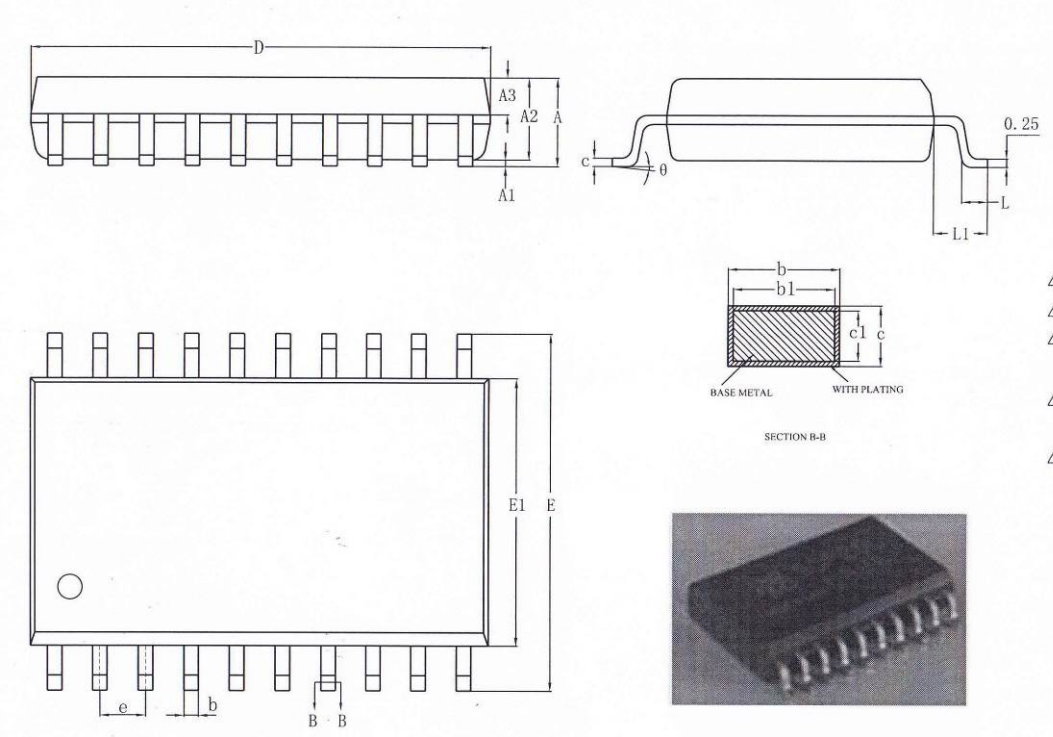


Figure 28 Switching Time Definition

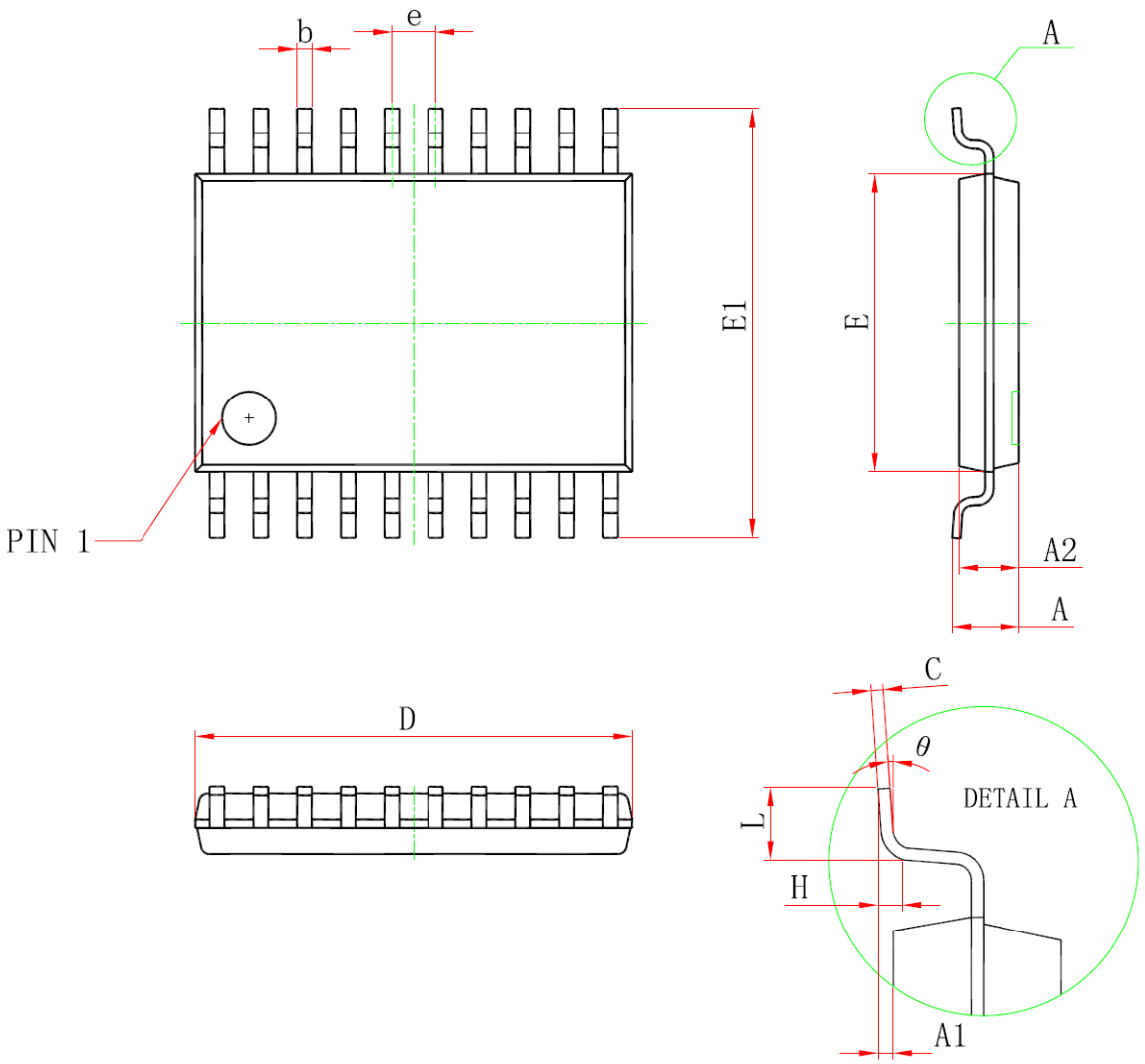
PACKAGE CASE OUTLINE

SOIC-20L (WB)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
⚠ b	0.35	—	0.43
⚠ b1	0.34	0.37	0.40
⚠ c	0.25	—	0.29
c1	0.24	0.25	0.26
⚠ D	12.70	12.80	12.90
E	10.10	10.30	10.50
⚠ E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	—	1.00
L1	1.40REF		
θ	0	—	8°

TSSOP-20L (NB)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Revision History

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.7 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Remove “June 2019”
Rev 1.8 datasheet, 2019-12-19	
Page 2	Change order information for SLM7888MD